BE (IT) Part IV 7th Semester Examination 2011

IT705/1: CAD for VLSI

Answer any SEVEN.

FM – 70 *Duration: 3 hr*

1. What are the different steps involved in a VLSI design cycle? Describe briefly with clearly mentioning the objectives at each level.

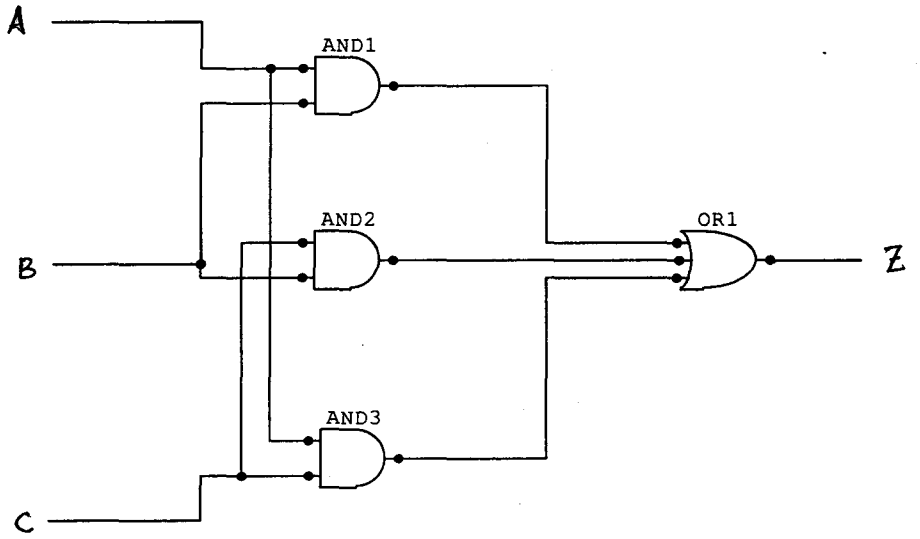
3+7

2. What are the Generic CAD tools associated with each design steps? Mention the CAD sub-problem levels also for these steps.

4+6

3.

   a. Mention different complexity metrics related to VLSI Physical Design. How do they vary for different design styles?
   b. Consider the following logic diagram of "full-adder carry" circuit. Let the inputs be A, B, C and the output be Z.
      i. Draw the connectivity graph for the following circuit.



   c. Represent the connectivity matrix for the same.

(2+3)+2+3

4. Give a general formulation of the floorplanning problem. How does this differ from the placement one? Give an Integer programming based floorplanning problem formulation with fixed blocks only.

2+2+6

5. What are center to center and HPWL estimations of wirelength? What are the objectives of a good placement? Give a general formulation of the placement problem. How does this vary with different design styles?

3+2+3+2

6. What is different partitioning based placement procedures? Describe quadrature placement and bisection placement procedure briefly.

4+3+3

7. Classify different types of placement algorithms. Name some simulation based algorithms. How simulated annealing may be applied to obtain a good placement? Describe briefly.

2+2+6

8. A net is represented by the following graph. G=G(V,E), where, V={1,2,3,4,5,6,7,8} and E={(1,2), (1,5), (1,6), (2,5), (2,6), (3,6), (3,4), (3,7), (3,8), (4,7), (4,8), (5,6), (7,8)}. Apply the Kernighan-Lin heuristic to optimize the partition. Assume initial bisection as V1={1,2,3,4} and V2={5,6,7,8}. Clearly explain each step of operation.

10

9. What is grid routing? Classify different grid routing algorithms. Explain Lee's algorithm with a simple example.

2+2+6

10. What is a Steiner tree? What are the different design style specific issues in global routing? How does a channel intersection graph model differ from the checker board model? Explain.

2+3+5