B.E. (IT) Part-Ill, 6" Semester Examination, 2010

Advanced Computer Architecture

{IT-605)

Full Marks: 70 Time : 3 hours

Answer any 7 questions

1. (a) Discuss different MIPS addressing modes,
   (b) How do you load larger constants? 8 12

2. a) How do you define Performance?
   b) Compare performances of A and B machine. A runs a program in 20 seconds and machine B runs the same program in 25 seconds.
   c) If clock rate ~ 50 MHz. find execute time for a program with 1,000 instructions, if the CP1 for the program = 3.5? If clock rate increases from 200 MHz to 250 MHz and the other factors remain the same, how many times faster will the computer be?
   d) Two compilers being tested for 100 MHz machine with 3 classes of instructions:
      - A (1 cycle), B (2 cycles), and C (3 cycles)
      - Compiler 1: 5M A, IM B. 1M C instructions
      - Compiler 2: 10M A, 1M B, 1M C instructions

   Which sequence has higher MIPS? Which sequence has lower execution lime?

   1-KM 2+1+2+2

3. a) What is Amdahl's Law?
   b) A program runs in 100 seconds on a machine, with multiply responsible for 80%. How much do we have to improve the speed of multiplication if we want the program to run 4 times faster? How about making it 5 times faster?
   c) Suppose we enhance a machine making all floating-point instructions run five times faster. If the execution time of some benchmark before the floating-point enhancement is 10 seconds, what will the speedup be if half of the 10 seconds is spent executing floating-point ' instructions? 2*2*2* 2+2

4. a) What are the basic components of data path implementing R-format instructions?
   b) Explain & draw the simple single cycle data path for the MIPS architecture executing the basic instructions load/store word. ALU operation and branch operation. 2+7

5. The operation times for the major functional units in single cycle implementation are the following: (1) memory' units: 2 ns. (2) ALU and adders: 2 ns. (3) Register file (read or write): Ins

   Assuming that the multiplexers, control unit, PC accesses, sign extension unit, and wires have no delay, which of the following implementations would be faster and by how much?
   i) An implementation in which every instruction operates in I clock cycle of a fixed length.
   ii) An implementation where every instruction executes in 1 clock cycle using a variable-length clock, which for each instruction is only as long as it needs to be. To compare the-performance, assume the following instruction mix: 24% loads. 12% stores, 44% ALU instructions, 18% branches, and 2% jumps. 10

6. a) Write different control inputs for Single cycle MIPS processor in tabular form,
   b) Calculate the delay for the instructions {add, sub, and. or, sit, sw. Iw, bcq. j}

   5+5

7. a) What are the problems with single cycle design?
   b) How do you calculate the clock period for single cycle and multi-cycle design?
   c) Draw the block diagram implementation for Multi-cycle approach. 3'3+4

K. a) How is the resource utilized in single cycle design, multi-cycle design, pipeline design?
   b) Draw cycle time and CP! lor different implementations.
   c) Draw the abstract model of pipelined data path. 3+3+4

9. a) What is Pipeline hazard?
   b) What are the different types of pipeline hazards?
   c) Discuss one type of pipeline hazards and what are the possible solutions to remove this . hazard? M 3ˢ 6

10. a) Define Instruction-I .evcl-parallelism and processor-level-parallclism.
    b) What are ***diffcrcnl*** types of Processor organizations according to Flynn's classification?
    c) What are the four potential advantages of SMP processor? 2+4+4

11. Short notes (any two) (2 x 5)
    a) Array Processor
    b) Vector Processor
    c) 16-bit CLA adder using 2 levels of look ahead
    d* Booth's algorithm for multiplication
    c) Instruction formats in MIPS