6th Semester B.E. (Information Technology), Final Examination 2012

Advanced Computer Architecture (IT-605)

Full Marks-70 **Time: 3 hours**

Answer any seven questions

1. a) How are Byte-addressable memories organized in MIPS?
   b) Suppose that $s0 initially contains 0x23456789. After the following program segment is run on a big-endian system and a little-endian system, what value does $s0 contain? lb $s0, 1($0) loads the data at byte address (1+ $0)= 1 into the least significant byte of $s0.

```
sw $s0, 0($0)
lb $s0, 1($0)
```

   c) In MIPS programs, at which starting address are the MIPS Instructions normally stored?
   d) Translate the following machine language code into assembly language.
      i) 0x2237FFF1
      ii) 0x02F34022 2+3+1+4

2. a) What are the differences between PC-Addressing and Base Addressing Modes?
   b) Why is the 'MIPS direct addressing mode' called 'Pseudo-direct Addressing'? 4+3+3
   c) If the JTA of the jal instruction is 0x004000A0, derive the 26-bit address field (addr) of this jal instruction.

3. a) What are the different Instruction formats in MIPS Architecture? Explain each type of formats.
   b) What is MIPS address space?
   c) How does MIPS architecture divide the address space into four segments? 5+1+4

4. a) What is Amdahl's Law?
   b) A program runs in 100 seconds on a machine, with multiply responsible for 80%. How much do we have to improve the speed of multiplication if we want the program to run 4 times faster? How about making it 5 times faster?
   c) Suppose we enhance a machine making all floating-point instructions run five times faster. If the execution time of some benchmark before the floating-point enhancement is 10 seconds, what will be the speedup if half of the 10 seconds is spent executing floating-point instructions? 2+2+2+2+2

5. a)What is the delay for the following types of 64-bit adders? Assume that each two-input gate delay is 150 ps and that a full adder delay is 450 ps.
   (i) a ripple-carry adder
   (ii) a carry-lookahead adder with 4-bit blocks
   (iii) a prefix adder
   b) Design a shifter that always shifts a 32-bit input left by 2 bits. The input and output are both 32 bits. Explain the design in words and sketch a schematic. 6+4

6. a) Implement the following functions using a single 16 x 3 ROM. Use dot notation to indicate the ROM contents.
   i) $X = AB + BC'D + A'B'$
   ii) $Y = AB + BD$
   iii) $Z = A + B + C + D$
   b) Specify the size of a ROM that you could use to program each of the following combinational circuits. Is using a ROM to implement these functions a good design choice? Explain why or why not.
   i) a 16-bit adder/subtractor with *C*in and *C*out
   ii) an 8 x 8 multiplier 6+4

7. a) Write different control inputs in tabular form for single cycle data path implementing MIPS Architecture.
   b) Calculate the delay for the instructions {add, sub, and, or, slt, sw, lw, beq, j}. 5+5

8. a) The operation times for the major functional units in single cycle implementation are the following: (1) memory units: 200 picoseconds (ps), (2) ALU and adders: 100 ps, (3) Register file (read or write): 50 ps
Assuming that the multiplexers, control unit, PC accesses, sign extension unit, and wires have no delay, which of the following implementations would be faster and by how much?
(i) An implementation in which every instruction operates in 1 clock cycle of a fixed length.
(ii) An implementation where every instruction executes in 1 clock cycle using a variable-length clock, which for each instruction is only as long as it needs to be. To compare the performance, assume the following instruction mix: 25% loads, 10% stores, 45% ALU instructions, 15% branches, and 5% jumps.
b) What are the problems with single cycle design? 8+2

9. a) A CPU needs 50 ns for instruction fetch. Calculate performance improvement if instruction prefetch feature is included in the processor. Assume that 20% of the instructions are branch instructions.
b) A CPU has 1KB memory space. Design a four-way memory interleaving with memory ICs of 50ns cycle time and calculate the effective bandwidth. 5+5

10. a) How do you avoid the problems of single cycle data path?
b) How do you calculate the clock period for single cycle and multi-cycle design?
c) Draw the block diagram implementation for Multi-cycle approach. 3+3+4

11. a) Draw the abstract model of pipelined data path.
b) What are the different types of pipeline hazards?
c) Discuss one type of pipeline hazards and what are the possible solutions to remove this hazard? 3+3+4

12. a) Define Instruction-Level-parallelism and processor-level-parallelism.
b) What are the different types of Processor organizations according to Flynn's classification?
c) What are the four potential advantages of SMP processor? 2+4+4