B.E. (IT), Part-III, 5th Semester Examination, 2012

Subject: Microprocessors **Paper Code: IT-502**

Branch : Information Technology

Time: 3 hours **Full Marks: 70**

Answer 7 questions.

1. a) Explain with the diagram the de-multiplexing scheme of the Bus AD_7-AD_0 in 8085.
   b) Draw the 8085 Timing Diagram for Execution of Instruction MVI A, 47H.
   c) Discuss the use of READY pin of the 8085 CPU. 4+4+2

2. a) Define Instruction cycle, Fetch cycle, Execute cycle, Machine cycle.
   b) What are the functions of status signal S_0 and S_1?
   (c) In which addressing mode do the following instructions belong?
   (i) LXI H, 2000, (ii) STA 2001, (iii) RAL, (iv) DAD rp.
   6+2+2

3. a) What are the functions of Instructions EI, DI , SIM and RIM?
   b) The microprocessor is completing an RST 7.5 interrupt request and RST 6.5 is pending. Write down the necessary program to check whether it is pending and if it is pending, enable RST 6.5 without affecting any other interrupts, otherwise, and return to the main program. 6+4

4 a) Show how the contents of each of the registers & the memory locations vary after execution of each of the following instructions.

	A	B	C	D	E	H	L	1000	1001	1002	1003	1004
Initial	35	28	41	10	02	25	00	27	25	37	41	56
LDAX D												
XCHG												
MVI M, 56H												
MVI A, 25H												
MOV C, D												

(b) Sixteen bytes of data are stored in memory locations at XX50 H to XX5F H. Write a suitable program to transfer the entire block of data bytes to new memory locations starting at XX70H.
5+5

5. a) What do you mean by software & hardware interrupts in microprocessor? Explain the interrupt facilities in 8085 microprocessor.
   b) Give the vectored addresses of eight software interrupts?
   c) What is ISR and how does it work? 2+4+4

6. a) What is Bus Contention?
   b) Compare the advantages and disadvantages of fully decoded memory interface scheme with the partially decoded scheme.

(c) MPU system requires 4k bytes of ROM and 4k bytes of RAM and both the devices are available in 2kx8 organization. Design a (i) fully decoded memory interface assuming RAM contiguously on the higher order address space and ROM on the lower address space (ii) partially decoded memory interface. Write down the corresponding memory map. 2+ 4+ 4

7. a) Differentiate between memory mapped I/O & I/O mapped I/O.
   b) Discuss the operating modes of 8255 programmable peripheral interface.
   c) Write down the format for control word of 8255 PPI chip. 2+4+4
8. a) Briefly explain the functions of BIU and EU of 8086-μp.
   b) Explain the concept of segmented memory? What are its advantages? 5+3+2
9. a) Discuss a typical maximum mode 8086 system.
   b) What is the difference between the jump and loop instructions?
   c) Write a program to find out the largest number from an array of sixteen 8-bit numbers stored sequentially in the memory locations starting at offset 0300H in the segment 3000H. 3+2+5
10. a) What are the functions of IP and SI registers in 8086?
    b) Explain Indexed Addressing and Based Indexed Addressing modes in 8086 microprocessor.
    c) Add the contents of the memory location 3000H: 0300H to contents of 4000H: 0400H and store the result in 5000H:0500H. 2+3+5

11. Write technical notes on (Any Four) 4 x 2.5=10
    a) Static and Dynamic RAM
    b) Asynchronous Data Transfer
    c) Design a memory system of size 4K bytes using chips of size 2Kx 4 bits.
    d) Control word format for BSR (Bit Set/Reset) Mode
    d) Function of SOD and SID Pin in 8085
    e) Stack operation and stack related instructions.
    f) Function of DAA instruction in 8085
    g) Physical address formation in 8086