B.E (ETC) 7th Semester Final Examination, 2013
Subject: VLSI Logic Design (ET 706/3)

Time: 3 hours **Full marks: 70**

Use separate Answer script for each half

First Half

Attempt ALL questions

1. Write down the CORDIC algorithm for both vectoring and rotation operation. Perform VLSI design for a serial CORDIC processor for both operations. Explain also the various sub-blocks used in this design. (10)

2. Write notes on
   (i) Four bit parallel unsigned binary divider
   (ii) Built in self test in VLSI (10)

3. (a) Explain with the help of flow chart the various steps in VLSI design flow.
   (b) Design an additive array multiply module to implement following function
   $P=AXB + C + D$
   ($A=a_3\ a_2\ a_1\ a_0$, $B=b_1\ b_0$, $C= c_3\ c_2\ c_1\ c_0$, $D= d_1\ d_0$) (15)

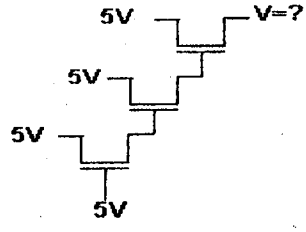
Second Half

Attempt ALL questions

4. Choose the correct alternative

A) Threshold voltage (Vt) of MOSFET
i) Increases with increased doping and decreases with decreased oxide thickness
ii) Increases with increased doping and increases with decreased oxide thickness
iii) Decreases with increased doping and decreases with decreased oxide thickness
iv) Decreases with increased doping and increases with decreased oxide thickness

B) Assume V_T=1V



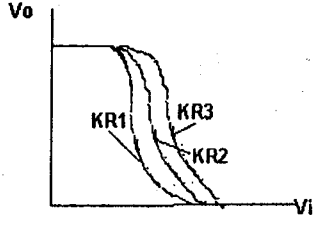
i)2V ii) 1V iii) 3V iv) 4V

C) In constant voltage scaling
i) Power dissipation increases and power density decreases
ii) Power dissipation decreases and power density increases
iii) Power dissipation decreases and power density remain same
iv) Power dissipation remain same and power density decreases

D) Threshold voltage (Vt) of MOSFET

i) Decreases for short channel effects and increases for narrow channel effects
ii) Increases for short channel effects and decreases for narrow channel effects
iii) Decreases for short channel effects and decreases for narrow channel effects
iv) Increases for short channel effects and increases for narrow channel effects

E) For a CMOS Inverter



i) $K_{R1}=4.0, K_{R2}=1.0, K_{R3}=0.25$
ii) $K_{R1}=1.0, K_{R2}=0.25, K_{R3}=4.0$
iii) $K_{R1}=0.25, K_{R2}=1.0, K_{R3}=4.0$:Where $K_R=K_n/K_p$ 5x1=5

5. a) Amongst a CMOS NAND and NOR gate which one is better and why?
b) Discuss the voltage transfer characteristics of CMOS inverter with emphasis on region of operation of n-MOS and p-MOS.
c) What is the advantage of transmission gate logic over pass transistor logic?
5x3=15

6. a) What is drain induced barrier lowering?
b) How the problem of conventional dynamic circuit is circumvented by Domino logic?
c) Discuss the purpose of weak pull up transistors in Domino CMOS logic
5X3=15