Bengal Engineering and Science University, Shibpur
B.E. 7th SEMESTER (ETC) FINAL EXAMINATION, 2012
VLSI Logic Design (ET-706/3)

Time: 3 hours Full marks: 70

Use Separate Answer Script for each half

First half

(Answer question number 1 and any One from the rest)

1. (a) Explain with circuit diagram the operation of 5 bit signed binary array multiplier.
(b) Design a arbitrary counter using D flip flops which will generate the sequence 2, 7, 10, 11, 6, 8 and repeats thereafter. (15)

2. (a) Write down the CORDIC algorithm for both vectoring and rotation operation. Perform VLSI design for a serial CORDIC processor for both operations. Explain also the various sub-blocks used in this design.
(b) Explain with examples, different types of logic hazards? How to minimize them? (20)

3. (a) Write down the decimation-in-frequency FFT algorithm with 8 point signal flow graph. Describe the operation of a parallel FFT processor using above mentioned algorithm. Make a comparison between serial and parallel FFT processor. (20)

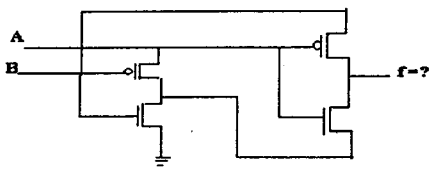
Second half

(Answer question number 8 and any two from the rest)

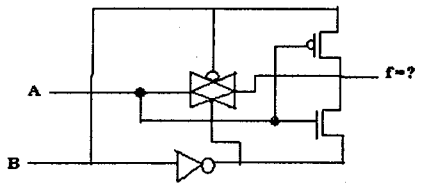
4. a) Amongst CMOS NAND and NOR gate, which one is better and why?
b) Discuss the relative merits and demerits of constant field scaling and constant voltage scaling. (15)

5. a) Discuss the operation of the circuits shown below and find 'f'.

i)



ii)



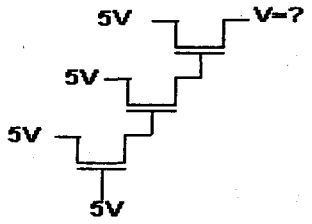
b) Differentiate between short channel and narrow channel effect. (15)

6. a) Discuss the operation of dynamic logic? What are the problems of these circuits and how that can be circumvented by Domino logic?
b) Discuss the role of weak pull up transistor in minimizing charge leakage of domino logic. (15)

7. a) Discuss the following i) Substrate Current Induced Body effect ii) Punch through iii) Hot carrier degradation.
b) Implement XOR gate using Complementary Pass Transistor Logic. (15)

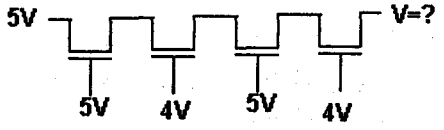
8. Choose the correct alternative

a) Assume V_T=1V



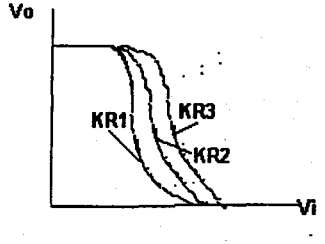
i)2V ii) 1V iii) 3V iv) 4V

b) Assume V_T=1V



i)2V ii) 1V iii) 3V iv) 4V

c)



i) K_{R1}=4.0,K_{R2}=1.0,K_{R3}=0.25
ii) K_{R1}=1.0,K_{R2}=0.25,K_{R3}=4.0
iii) K_{R1}=0.25,K_{R2}=1.0,K_{R3}=4.0 :Where $K_R=K_n/K_p$

d) In saturation region of a MOS
i) Static resistance is high, dynamic resistance is low
ii) Static resistance is low, dynamic resistance is high
iii) Static resistance is high, dynamic resistance is high
iv) Static resistance is low, dynamic resistance is low

e) LDD structure is used to reduce
i) Channel length modulation
ii) Hot carrier degradation
iii)DIBL
iv) GIDL

1x5=5