Bengal Engineering and Science University

Final-Sem Examination 7th Sem E&T.C. 2013, Dec.

Sub: Electronics Design Automation (ETC-703) Time: 3 Hours Full Marks: 70

Answer any five questions.

1. a) Briefly outline the purposes of the following VHDL modeling constructs: (i) entity declaration (ii) behavioral architecture body (iii) structural architecture body (iii) process statement (iv) signal assignment (v) port map, (vi) Array type, (vii) Concurrent statement.

2. a) Write an entity declaration and a behavioral architecture body for a two-input multiplexer, with input ports a,b and sel and an output port z. If the sel input is '0' the value of 'a' should be copied to 'z', otherwise the value of 'b' should be copied to 'z'. Also explain the function of the each statements used in architecture and entity declaration body.

   b) Write the data flow description of a 1 bit comparator. The output of the comparator becomes 1 when two inputs are equal

3. (a) Write variable declarations for a counter, initialized to 0; a status flag used to indicate whether a module is busy; and a standard-logic value used to store a temporary result.
   (b) Write the VHDL code for the full adder using only two-input NAND gate.

   (c) Write the data flow description for a bit subtracter. Include a borrow input and borrow output.

4. Circuit shown in the figure represents schematic diagram of an operational amplifier. Write the SPICE code for the circuit to compute the frequency response characteristic of the circuit. Output of the circuit should be displayed in graphics mode.

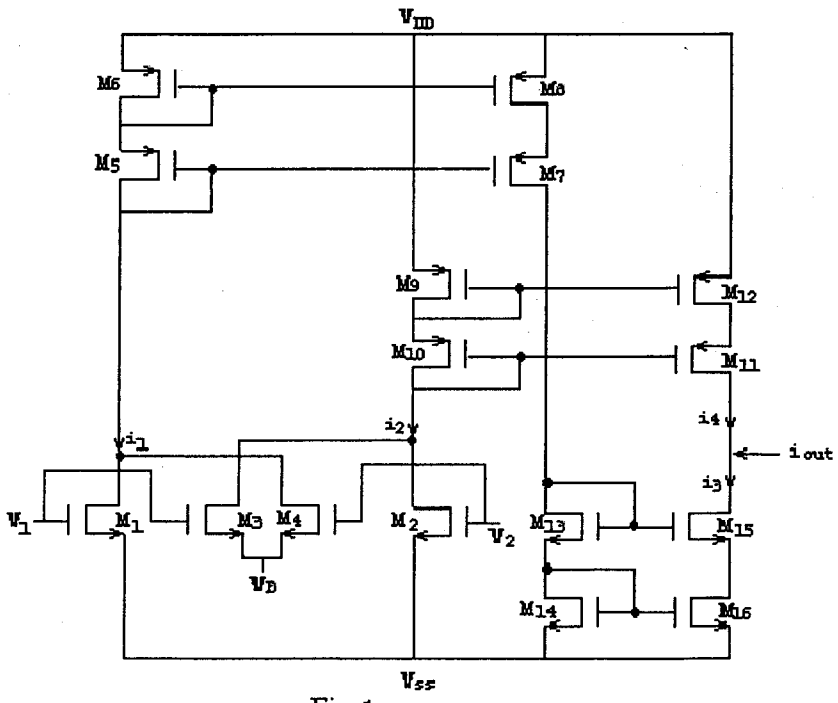
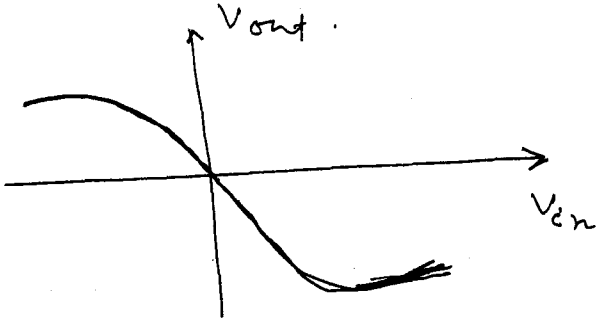


Fig. 1

5. a) For a square law MOS transistor operating in saturation, the chrematistic of the curve shown below can be expressed as, $V_{out} = -\frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{in}\sqrt{(\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - V_{in}^{\ 2}R_D)}$. If the differential input is small, approximate the characteristic by a polynomial.



b) Write VHDL code for for a counter with an output port of type natural, initially set to 12. When the clk input changes to '1', the decrements by one. After counting down to zero , the counter wraps back to 12 on the next clock edge. Also explain the design procedure of the counter with the necessary diagram.

6. a) Two nonlinear stages are cascaded. If the input / output characteristic of each stage is approximated by third order polynomial, then discuss the non linearity effect of the syatem.

b) State the differences between transport delay and inertial delay.

7. Describe the implication chart method with an suitable example.

8. Write short note on:
(i) Simulation deltas.
(ii) Time analysis of digital system
(iii) Device modeling .