BENGAL ENGINEERING AND SCIENCE UNIVERSITY, SHIBPUR
7th Semester B.E.(ETC) Examination 2012
ELECTRONIC DESIGN AUTOMATION
Subject code: ET 703

Total Marks:70 **Time: 3hours**

Answer any seven questions

1. a) State the advantages of using Signals and Variables in VHDL programming
b) Design a circuit of a four Bit parallel adder using structural modeling style in VHDL.
c) With suitable examples briefly define the use of functions and subprograms in VHDL.
[3+3+4 = 10]

2. a) Describe the following front end design steps for ASIC design
i) Specification ii) Logic synthesis iii) Functional verification.
b) State the significance of layout in context of physical design of an ASIC.
[6+4 = 10]

3. a) A 180 nm standard cell process can have an average switching capacitance of 150 pF/mm^2. A chip is composed of random logic with an average activity factor of 0.2. Estimate the power consumption of the chip if it has an area of 70 mm^2 and operates at 450 MHz at V_{DD}=0.9 V.
b) To save power in a static CMOS gate, V_{DD} can be reduced and at the same time V_t is also scaled. Under these circumstances what will happen to the static and dynamic power consumption? **[5+5=10]**

4. (a) Draw the Q-V characteristics of an ideal MOS capacitor? Explain these characteristics briefly? Formulate an expression for the accumulation charge, depletion charge and the inversion charge in these characteristic curves.
(b) Formulate an expression for the threshold voltage of an ideal MOS capacitor.
[6 +4=10]

5. (a) Sketch the electron density profile along the length of a n-channel MOSFET, moving from source to drain? Explain briefly the nature of the profile?
(b) Derive an expression for the drain current of a n-channel MOSFET assuming that the MOSFET is operating above threshold. Calculate the drain voltage for which the drain current is maximum hence find the value of the saturation current.
[4+6=10]

6. A string of inverters is used to drive a signal that goes off-chip through a pad. The capacitance of the pad and its load is equivalent to 20,000 microns of gate capacitance. Assuming the driver is a unit-sized inverter in a 0.6μm process with 7.2 microns of input capacitance, how should the inverter string be designed? **[10]**

7. A path has to be designed here to drive the enables of a bank of 64 tri-state bus drivers. The first stage of the path presents an input capacitance of 12 unit-sized transistors. Each tri-state driver is 6 times the unit sized tri-state inverter. A unit sized tri-state inverter is shown in Figure 1.

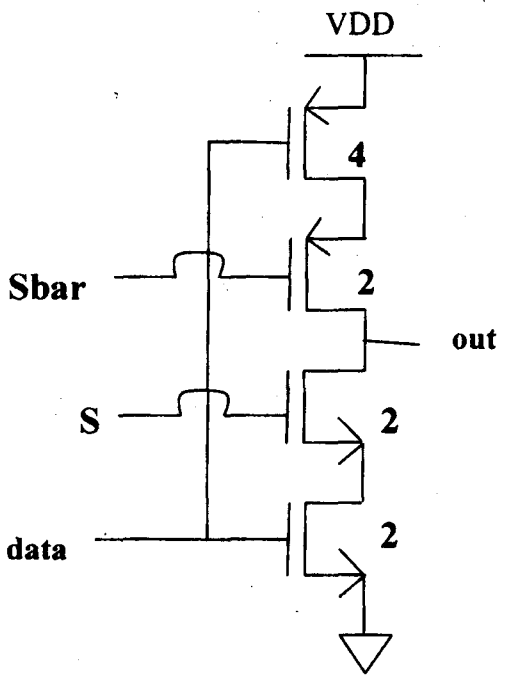


Figure 1: A unit-sized tri-state inverter. Sbar is the complement of S.

Design the path using a 2-3 fork structure as shown in Figure 2. **[10]**

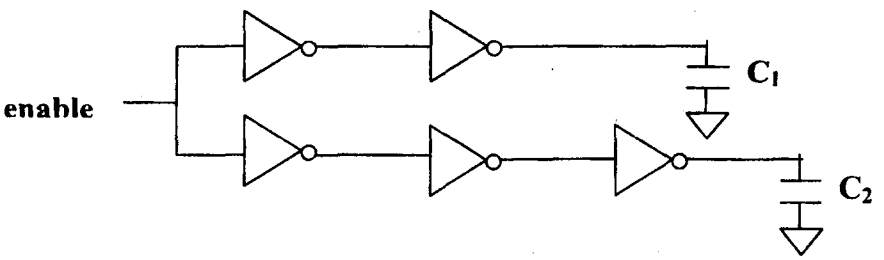
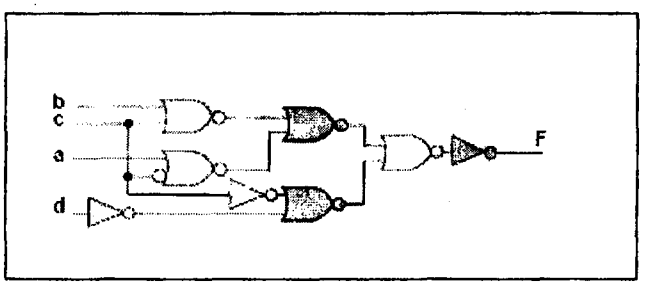


Figure 2 : A 2-3 fork structure.

8. Find all the Hazards in the circuit given below at output F. Describe all the necessary steps in details with explanations. **[10]**



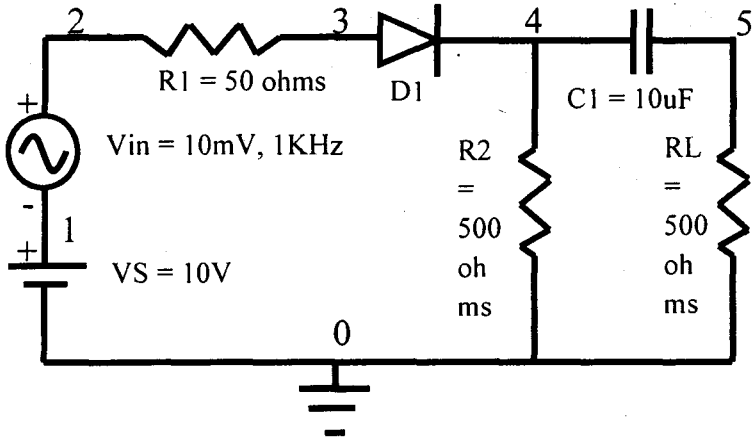
9. With respect to high-level synthesis from the program-code as following(high-level specification) derive the datapath and the final controller, show all the steps in details with necessary diagrams and proper explanation.

```
x<= a + b ;
 y<= a * c ;
z<= x + d ;
x <= y – d ;
x <= x + c ;
```

[10]

10.a) What are the different types of analyses that can be performed in SPICE? Write the corresponding statements in SPICE.

b) Write the SPICE netlist for a series diode clipper shown below to perform transient analysis for a suitable time. Plot the waveform at node 5.



[4+6=10]