BENGAL ENGINEERING AND SCIENCE UNIVERSITY, SHIBPUR
B.E. 5TH SEMESTER (ETC) FINAL EXAMINATIONS, December 2012
SUB: INTEGRATED CIRCUITS and SYSTEMS (ET-502)

Full Marks: 70 **Time: 3 hrs**

ANSWAR Q. No. 1 and any three from the rest

(1) (a)

Set up a computer in block-diagram form, using operational amplifiers, to solve the following differential equation:

$$\frac{d^3y}{dt^3} + 2\frac{d^2y}{dt^2} - 4\frac{dy}{dt} + 2y = x(t)$$

where

$$y(0) = 0 \qquad \left.\frac{dy}{dt}\right|_{t=0} = -2 \qquad \text{and} \qquad \left.\frac{d^2y}{dt^2}\right|_{t=0} = 3$$

Assume that a generator is available which will provide the signal $x(t)$.

(b) Design 1 no 64X4 RAM BLOCK using 16 no 16X1 RAM BLOCKs (having write enable input) and logic gates.
(c) Design a full adder using multiple no of 2:1 MUX blocks only (25)

(2) Define (i) CMRR (ii) Slew rate (iii) Input offset voltage (iv) Output offset voltage of an OP-AMP. How to nullify input offset voltage of an OP-AMP in non inverting amplifier configuration. Derive the expression of active RC bandpass filter with necessary circuit diagram (15)

(3) Describe with circuit diagram application of an OP-AMP as a (i) antilogarithmic amplifier (ii) fast full-wave rectifier (iii) relaxation oscillator (iv) triangular wave generator (15)

(4) Describe with all necessary circuit diagrams the operation of a voltage to frequency converter. How an A/D converter can be realized using this. Explain the operation of 4 bit pipelined A/D converter with necessary diagrams. (15)

(5) What are the relative merits and demerits between FPGA and ASIC. Draw and explain CLB of XILINX SPARTAN FPGA. How to realize a dual port RAM using CLB of FPGA. (15)

(6) Write notes on
(i) Switched capacitor filter
(ii) 555 timer as astable multivibrator
(iii) Static RAM cell using BJT. (15)