Bengal Engineering and Science University, Shibpur
B.E ETC 7th Semester Examination, 2011
VLSI Logic Design (ET 706/3)

Time: 3 hours **Full marks: 70**

Part-A
(Answer question number 1 and any One from the rest)

1. (a) Explain with examples, different types of logic hazards? How to minimize them?
(b) Design an additive array multiply module to implement following function
$P=AXB + C + D$
($A=a_3\ a_2\ a_1\ a_0$, $B=b_1\ b_0$, $C= c_3\ c_2\ c_1\ c_0$, $D= d_1\ d_0$) (15)

2. (a) Write down the CORDIC algorithm for both vectoring and rotation operation. Perform VLSI design for a pipelined CORDIC processor for both operations. Explain also the various sub-blocks used in this design.
(b) Explain with circuit diagram the operation of Four bit parallel unsigned binary divider. (20)

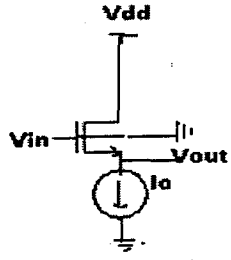
3. (a) Write down the decimation-in-frequency FFT algorithm with 8 point signal flow graph. Describe the address generation block for the abovementioned algorithm.
(b) Design a arbitrary counter using D flip flops which will generate the sequence 2, 9, 7, 11, 5, 8 and repeats thereafter. (20)

Part-B
(Answer question number 5 and any two from the rest)

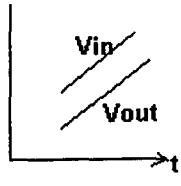
4. [Choose the correct alternative]

a) Threshold voltage (Vt) of MOSFET
i) Increases with increased doping and decreases with decreased oxide thickness
ii) Increases with increased doping and increases with decreased oxide thickness
iii) Decreases with increased doping and decreases with decreased oxide thickness
iv) Decreases with increased doping and increases with decreased oxide thickness

b)



For body bias effect input and output voltage relation is like

i)


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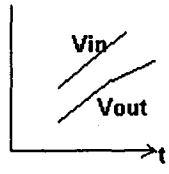

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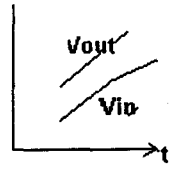

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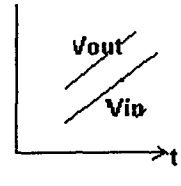


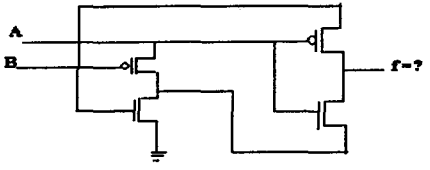
c) In saturation region of a MOS
i) Static resistance is high, dynamic resistance is low
ii) Static resistance is low, dynamic resistance is high
iii) Static resistance is high, dynamic resistance is high
iv) Static resistance is low, dynamic resistance is low

d) Switching Threshold voltage of CMOS inverter
i) Increases ii) Decreases iii) First decreases then increases iv) remain unchanged with increasing transconductance ratio (kn/kp).

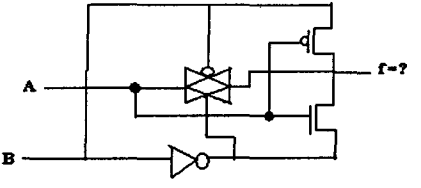
e) If initial doping density is NA then after constant voltage scaling it becomes (S=scaling factor)
i) SN_A ii) S^2N_A iii) S^3N_A iv) Remain same. 1x5=5

5. a) Amongst a CMOS NAND and NOR gate which one is better and why?
b) Discuss the factors on which threshold voltage of MOS transistor depends.
c) Derive the expression for switching threshold voltage of the CMOS NOR2 gate
4+5+6=15

6. a) Discuss the operation of the circuits shown below and find 'f'.
i)



ii)



b) What is the problem of pass transistor logic and how that problem can be solved?
9+6=15

7. a) Discuss various voltage dependent capacitances of MOSFETs. In which region (s) MOS offers the maximum capacitance and why?
b) How the linearity of the switch capacitor circuit can be improved? 8+7=15