Bengal Engineering and Science University, Deptt. of E&T.C.

Final Sem Examination 2011

7th Sem E&T.C.

Subject: Electronics Design Automation (ET-703)

Time: 3 Hours **F.M. 70**

Answer any three questions from each group. All questions carry equal marks. Two marks, from each half, are reserved for neatness and to the point answer. Answer all questions in a single answer script.

FIRST HALF

1. (a) Fig. 1 depicts the state diagram of sequence detector. Analyze the state diagram and write a VHDL description for the sequence detector , 110 .

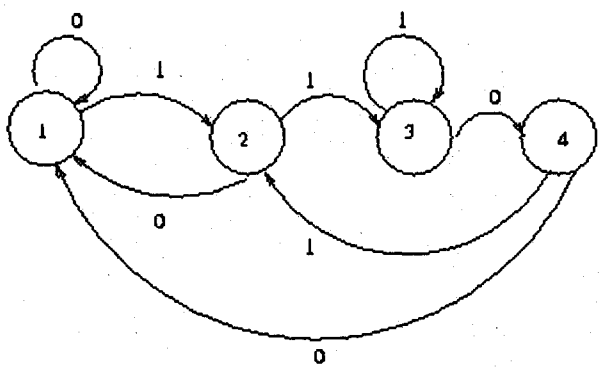

Fig. 1

(b) What do understand by hardware simulation? Explain in details.

2. (a) State the difference between events and transactions.
   (b) Write the VHDL description of single bit comparator.
3. (a) Write a counter model with a clock input clk of type bit, and an output q of type integer. The behavioral architecture body should contain a process that declares a count variable initialized to zero. The process should wait for changes on clk. When clk changes to '1', the process should increment the count and assign its value to the output port.
   (b) List all the tran sactions in the following description. State reason and justifications for each transaction. No credit will be gives without justification).

```
ARCHITECTURE sequential of timing_demo Is
  SIGNAL a,b,c : BIT := '0';
  BEGIN
  PROCESS
  BEGIN
  a <= '1' ;
  b <= NOT a,
  c <= NOT b ;
  WAIT ;
```

END PROCESS;
END sequential;

4. (a) Draw the design flow diagram of an VLSI chip, and explain the function of each .step

(b) Discuss the requirements that led to the design of VHDL language. Which of these requirement exists in C languages? Considering these requirements, discus where a software language would fall short in describing hardware.

5. Write short notes on:
(a) MOS modeling in SPICE
(b) Delta delay
(c) Transport delay and Inertial delay

SECOND HALF

6. (a) State the differences between combinational and sequential digital circuit.
(b) A long sequence of pulses enters a two-input two-output synchronous sequential circuit, which is required to produce an output pulse z =1 whenever the sequence 1111 occurs. Overlapping sequences are accepted; for example, if the input is 01011111....., the required output is 00000011...
(a) Draw state diagram.
(b) Select an assignment and show the excitation and output tables.
Write down the excitation functions for SR flip-flops, and draw the corresponding logic diagram.

7. Let's consider a sequence-detecting finite state machine with the following specification. The machine has a single input X and output Z. The output is asserted after each 4-bit input sequence if it consists of one of the binary string 0110 and 1010. The machine returns to the reset state after each 4-bit sequence. Reduce that 4-bit string recognizer using implication chart method.

8. (a) Consider a circuit that solves numerically (by means of the backward Euler method) the following differential equation: $y'' + 3.x.y' + 3 = 0$ in the interval [0,a] with step size dx and initial values $x(o) = x$; $y(0) = y$; $y'(0) = u$. Draw the data-flow graph with necessary explanation.
(b) What do you mean by optimization techniques? Explain each type optimization technique in brief.

9. (a) A synchronous 3-bit counter has a mode control input m. When m = 0, the counter steps through the binary sequence 000, 001, 010, 011, 100, 101, 110, 111, and repeat. When m= 1, the counter advances through the Gray code sequence 000, 001, 011, 010, 110, 111, 101, 100, and repeat. Draw the state diagram, with proper explanation for the counter.

(b) Explain Moore machine and Mealy machine. Discuss the deferences between them.

10. Write short note on:
(i) Abstract models
(ii) Sequencing graph
(iii) Device modeling