B.E. (ETC) Part-Ill 6th Semester Examination, 2010

Advanced Microprocessor and Computer Architecture

(ET-602)

Time : 3 hours **Full Marks : 70**

Use separate answerscript for each half.
Answer SVC questions, taking THREE from each half.
The questions are of equal value.
Two marks are reserved for neatness in each half.

FIRST HALF

1. Draw and explain block diagram of 8086 based microcomputer system. Describe the basic 8086 system timing diagram. **[11]**

2. Describe the following 8086 instructions and assembler directions with examples: (i) Assume, (ii)AAM, (iii)LODSB, (iv)STD, (v)PTR, (vi)XCHQ (vii) ROR, (viii) XLATB, (ix) PUBLIC, (x) EXTRN. [II]

3. Draw and explain 8254 internal block diagram. Describe the 8254 control word format. Explain the 8254 MODE 1 operation with necessary timing diagram, [ill

4. Describe the protected mode of memory operation in 80286 microprocessor. Explain the memory paging mechanism in 80386 microprocessor. **|11I**

5. Draw and explain 80486 internal block diagram. What are the differences between 80286 and 80486 microprocessors? **|11]**

SECOND HALF

6. Describe Pentium microprocessor architecture with necessary diagram. Explain how instruction pipelining is done in Pentium. Explain the branch prediction mechanism. **[11]**

7. Draw a three-bus organization of a datapath with annotation. Write control sequence for the instruction Add R4, R5, R6 and explain it with respect to above mentioned datapath. **[11]**

8. Explain hardwired control unit organization showing decoding and encoding functions. How encoder generates the control signal for a processor and implemented with logic circuit for the step action. 1**11**J

9. How control signals required inside the processor can be generated using micro instructions? How the above organization can be modified to microinstructions with nest address field? **[11]**

10. What is pipelining used in a computer? A computer has 4-stage pipeline having four steps Fetch (F), Decode (D), Execute (E) and Write (W). Explain sequence of operation for four instructions. Explain the effect of an execution operation taking more than one clock cycle. **[11]**