B.E. (ETC) Part-II 4th Semester Examination, 2010

Digital Electronics
(ET-402)

Time : 3 hours Full Marks : 70

Answer gnu FIVE questions.

1. a) Derive the truth table of a binary full subtractor and write down the related logic expressions. Realize the same using only 2:1 MUX as a basic building block.

   b) Design a variable right shifter which can make a signed shifting of amount 0 to 7 bit of its 8 bit input data. The circuit should be combinatorial only. **[14|**

2. Design an additive array multiply module using full adder blocks only which can realize the following expression

   P = A x B + C + D

   where A is 4 bit (a_3, a_2, $a_{(1}$ a_0), B is 2 bit ($b_{1(}$ b_0), C is 4 bit (cj, c_2, $c_{1?}$ Co) and D is 2 bit (di, d_0) binary numbers. 114]

3. a) Using a neat circuit diagram exp'a'n the rderation of J-K flip-flop.

   . b) Design an arbitrary counter using D flip-tlop and logic gates which will generate 0, 5, 3, 4, 7 and repeats thereafter. 1I4J

4. a) Describe with necessary circuit diagram the operation of a 4-bit controlled adder/subtractor using two's complement number system. Explain with example how overflow condition is detected in this design.

   b) Design a pipelined fractional multiplier which scales its 16 bit input, DIN, as the following relationship

   DOUT = 0.707 x DIN [141

5. Explain the operation of a 4-bit unsigned parallel divider with necessary diagram. How this unsigned divider can be converted to signed divider. **[14]**

6. a) Design a 8:1 MUX using pass transistor logic. How a Boolean Function Unit can be realized using pass transistor logic.

   b) Describe with necessary circuit diagram the operation of integrated circuit DTL NAND gate. Derive the expression for its Fan-out. (141

7. Write notes on : [14]

   a) NOR gate realization using complementary MOS logic and it's stick diagram.

   b) Mealy machine,

   c) N-bit Serial Adder.