Time: 3 hrs   Full Marks: 70

Use separate answer script for each half
Answer Q. No1 and any two from the rest in First Half
Answer any *THREE* questions from Second Half
Two marks reserved for neatness in each half

FIRST HALF

1. Fill in the blanks with appropriate technical words.

   a) The clock frequency of the PIC Microcontroller in the High Speed Mode is………………..   [1]

   b) The size of the program memory for a PIC 16F877 microcontroller is ………………., the CPU of ……………. type and of an …………………. Architecture.   [3]

   c) The ………… signal checks whether the voltage has fallen below V_{dd} for a PIC Microcontroller   [2]

   d) The ……………… module helps to find out the time an event has occurred.   [2]

   e) In the …………… mode of the PIC microcontroller, the oscillator is put to rest.   [1]

   f) The two timers that enable the proper start-up of the PIC microcontroller are ………… and …………….   [2]

2. a) What do you mean by the principle of orthogonality? What is its role in digital signal processing?

   b) What do you mean by aliasing? What steps should be taken to prevent aliasing?

   c) Compute the DFT of the following signal x(n)={0,1,2,3}   [3 + 3 + 5]

3. a) Derive the matrix of twiddle function with regard to Discrete Fourier Transform.

   b) Why do you think the Digital Signal Processor Chip is most suited for digital filtering purpose?

   c) What is the difference between the FIR and IIR filters?   [6 + 2 + 3]

4. a) Draw the block diagram of the base architecture of the DSP chip ADSP2101 with a brief summary.

   b) What are odd and even functions?   [8 + 3]

5. a) Write a program in the Assembly Level Language for the ADSP2101 to compute the sum of the following series. $S=\sum r^n$ where n varies from 0 to N-1.   [11]

   <u>Or</u>

   b) Suppose the PIC microcontroller is being used to check the transition of a positive edge of a current signal from a zero crossing detector and the bit-0 of Port-A is being used as an Input port. The software will ensure that the positive edge of the input signal will be used to halt the program.   [11]

   [Use of a flowchart for either of the programs is appreciated]

6. a) What is the primary difference between a general purpose processor and a digital signal processor?

   b) Sketch the number line for a 16 bit fixed point processor. If the data format assumed is Q 1.14, then what is the range of decimal numbers that can be represented?

   c) If all numbers are represented in Q3 format, what is the sum of 0.625_D and 0.8125_D? Classify the error, if any and find its % value.

   d) What is sign extension? $[2 + (2 + 2) + 3 + 2]$

7. a) For a $\pm10V$ bipolar ADC, what digital value represents 3.6V analog input? How does this digital value change if the ADC is now connected to a fixed point DSP employing Q 2.13 format?

   b) Explain with a neat diagram how a DSP is used for sound recording in and reproduction from a compact disc

   c) What is 'Linear Predictive Coding' as applied to speech coding using DSP?
                                                      $[(2 + 2) + 4 + 3]$

8. a) Distinguish between the 'Data Link' and the 'Network' layers of the 7-layer OSI model? Ethernet is a protocol defining the behaviour of which layer? In this connection, explain CSMA/CD.

   b) What is the difference between a MAC address and an IP address? Explain with an example each.

   c) Distinguish among hub, switch and router. $[(2 + 1 + 2) + 3 + 3]$

9. a) What is meant by a 'hard' real-time embedded system? Give an example.

   b) What is an 'SoC'? What are its essential components?

   c) Realise a 2-bit digital comparator circuit in VHDL using dataflow / structural / behavioural mode (you may mix all three) of programming. $[2 + 4 + 5]$

10. a) Realize the following digital function in an FPGA:

    $$F = x + yz + xy$$

    b) What basic logic function is implemented in Actel (FPGA) logic module? Explain..

    c) In a hypothetical system having one state variable x_1 and one input u_1, if $dx_1/dt = 2*x_1 + u_1$ design an FPGA-based circuit to solve for x_1. Use any integration method. Show the timing details.
                                                  $[4 + 3 + 4]$