BE (EE) Pt-III 5th Semester Final Examination 2011
Subject : Solid State Devices and Circuits II
(EE 503)

Time : 3 Hours | Full Marks : 70

Use separate answerscript for each half
Answer SIX questions taking THREE from each half
Two marks are reserved for neatness in each half

FIRST HALF

1.(a) Derive the expression for higher cut-off frequency of a common-collector amplifier with resistive load.
(b) Explain the operation of a series-pass regulator using transistor based error amplifier. Explain fold back current limit. [4+7]

2. (a) Explain the operation of a transformer-coupled push-pull class B amplifier and calculate the maximum possible efficiency.
(b) Derive the expression for voltage gain in common source FET amplifier for high frequency operation. [6+5]

3. (a) With necessary circuit diagrams and waveforms, explain the operation of a single phase full-wave rectifier with center-tapped transformer. Calculate the rectification efficiency, ripple factor and transformer utilization factor.
(b) Write a brief note on three-pin voltage regulator. [7+4]

4.(a) Write short notes on capacitive and L-C filter used in power supply.
(b) Design the circuit of a voltage regulator using IC 723 for 5V output from 25 V dc input with a current limit of 1A. [6+5]

5.(a) Draw the functional block diagram of 555 timer IC and explain its operation as astable multivibrator.
(b) Explain different types of coupling methods for a multistage amplifier. [6+5]

SECOND HALF

6 (a) With the help of a block diagram, show the working principle of an oscillator using positive feedback. Give a list of at least five sinusoidal oscillator circuits. Describe with a schematic diagram operation of any one of the above oscillators. [6]

(b) Describe the operation of two ADC s one using V-T and another using V-f circuits. [5]

7 (a) With the help of circuit diagrams, show the differences between the R-S Latch and the R-S Flip-flop (F/F), both using NOR gates. What is a Contact De-bouncer circuit using a latch? [5]

(b) Develop the Preset (Pr) and the Clear (Cl) terminals in the R-S F/F and discuss functions of these terminals. Give a list of F/Fs and the different types of triggering techniques of the Clock (Ck) in F/Fs [6]

8 (a) Describe the construction and operation of 4-bit Buffer-Register using D-F/Fs, with LOAD (L) and ENABLE (E) terminals. (5)

(b) With the help of block diagram of a Bus-organized Register Structure containing 8-bit Buffer-Registers and write the sequential steps of the control-words in binary to LOAD two binary numbers in two registers and to interchange (SWAP) the contents in these registers. (6)

9 (a) Show that the Up-Down counting-modes of a Ripple Counter can be expressed in the terms of specification of the F/Fs and their external connections related by XOR-operators. (5)

(b) Design a Modulo-14 Up Ripple Counter considering the negative edge triggered T- F/Fs with Cl (CLEAR) terminals, as available in the stores. (6)

10 (a) With the help of Transition Diagram and Transition Table of a J-K F/F realize a T-only F/F, a T-F/F and D-F/F. (5)

(b) Design a non-sequential Synchronous Counter following the state diagram— (6)

(2)----(7)----(5)----(6)----(2)

and using J-K F/Fs, following Type-T design. Also show the Bush Diagram.