B.E. (EE) Part-II 4th Semester Examination, 2010

Solid State Devices and Circuits-I

(EE-404)

Time : 3 hours Full Marks : 70

Use separate answerscrjpt for each half.
Answer SIX questions, taking THREE from each half.
Two marks are reserved for neatness in each half.

FIRST HALF

1. a) Draw the Ebers-Moll model for a p-n-p transistor.

   b) Explain the output characteristic of a CB p-n-p transistor in the amplifying region with the help of the Ebers-Moll model.

   c) If both the junction is sufficiently reverse biased then prove that the emitter and collector current are given by

   $\backslash -a,a_N$ and $Ir = l-a,a_N$ [3+4+41

2. a) Define CE h-parameters.

   b) How do you measure experimentally the parameter $hj-_e'$?

   c) Find *hfo* in terms of CE h-parameters. [4+2+51

3. a) Find the small signal r.m.s. output voltage V_0 as shown in Fig.-1 due to low frequency excitation signal V_s- 10 mV r.m.s. The CE h-parameters values are h_{ie} = 1,100 h_n = *2.5* x 10~\ hf_e=50 and = 24*pAIV** The resistance values in the circuit are *, = 100K_y R_2= \0K, R_s= 1 * $_e$ = 1 K and = 1 *K*. The reactance values of the capacitances at the operating frequency can be considered to be zero.

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X

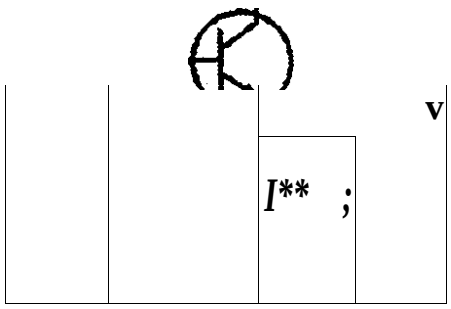

Fig.-l

b) Find the bias stability factor S (for variation of I_{CO}) for the same circuit assuming $P \ll I/I_c$. [7+41

4. a) Define g_m for a JFET.

b) Find the expression of g_m from the Shockley's equation.

c) Find the voltage gain and output resistance for a CS amplifier with source resistance. [3+2+61

5. a) Explain common mode signal and difference signal.

b) What is CMRR?

c) Explain the operation of an emitter coupled BJT difference amplifier and find the CMRR of the amplifier. J2+2+71

SECOND HALF

6. a) Define an operational amplifier (Op. AmpVOA). With the help of an equivalent circuit, represent an OA. What is an ideal OA? - Discuss the specification of an ideal OA.

b) Compare between actual ground point and virtual ground point, with the help of an amplifier circuit using OA, show these two ground points.

c) Draw a 3-point adder circuit using OA. Show the summing junction and derive the input-output relation. In this circuit, if the feedback resistor is replaced by a capacitor, what will be the analytical expression of the output? Name the circuit. [4+2+5]

7. a) With the help of a circuit diagram and analytical steps, discuss the operation of a differential input differential output circuit using OA. Suggest the single resistor gain control facility in it.

b) What is a zero crossing detector (ZCD)? Discuss the transfer characteristics of the circuit and describe the output waveform from the circuit if the input to the circuit is a 2 V peak to peak sinusoidal ac signal. |6+5]

8. a) Draw the circuit of a TTL inverter circuit with totempole active pull up circuit and describe its operation,

b) What is a CMOS inverting gate circuit? Show the internal circuit of a non-inverting gate in a CMOS logic family. (6+51

9. a) Prove that:

$AB + BC + CA = AB + BC + CA.$

Use truthtable, Venn diagram and K-map for proof.

b) Minimise the following function analytically and using K-map

$Y = Im(1,2,3,4,5,6)$

Draw the minimized circuit using NAND-NAND configuration. (5+61

10. Write short notes on anv two : **[5Kx2]**

a) Compare a passive-RC Integrator to its active counterpart using O.A,

b) Analog Regenerative Comparator and its application in an Astable Multivibrator.

c) Realisation of a Full Adder circuit using two-Half Adders and a gate.

d) Digital word comparator using Exclusive-OR gates.