BE (EE) Pt-III 5th Semester Final Examination 2013
Subject : Solid State Devices and Circuits II
(EE 503)

Time : 3 Hours | Full Marks : 70

Use separate answerscript for each half
Answer SIX questions taking THREE from each half
Two marks are reserved for neatness in each half

FIRST HALF

1.(a) Explain the operation of a transformer-coupled push-pull class B amplifier and calculate its maximum possible efficiency.
(b) Explain fold back current limit of a series pass regulator. **[6+5]**

2.(a) Derive the expression for α cut-off frequency of a common-base amplifier.
(b) Explain the operation of a buck converter and show that the output voltage is always less than the input voltage. **[5+6]**

3. (a) Derive the expression for voltage gain in a common source FET amplifier for high frequency operation.
(b) With necessary circuit diagrams and waveforms, explain the operation of a single phase half-wave rectifier. Calculate the rectification efficiency, ripple factor and transformer utilization factor. **[4+7]**

4.(a) Draw the functional block diagram of 555 timer IC and explain its operation as monostable multivibrator.
(b) Design the circuit of a voltage regulator using IC 723 for 5V output from 20V dc input with a current limit of 1A. **[7+4]**

5. Write brief notes on:
(a) Opto-coupler
(b) Inductive filter used in linear power supply **[6+5]**

SECOND HALF

6. a) With the help of circuit diagram and Status Table of the transistors, describe the operation of the 2-input TTL NAND gate with Open Collector(O.C.) output. Also discuss the advantages of this type of output hardware. State also the requirement of grounded reversed biased diodes connected to the input terminals.
b) Give the circuit diagram of the 2-input NOR gate in TTL logic family with Totempole output configuration, describe the operation of the output circuit. Now draw the transfer characteristics of this circuit considering this as an inverting gate.
[6+5]

7. a) Draw the circuit diagram of a 2-input CMOS AND gate and describe its operation. State the advantages and disadvantages of CMOS family.

b) What is a 2-input ECL OR-NOR gate circuit? Describe the operation of the circuit. State the advantages of this family and state why the grounded positive supply is used? Also mention the second power supply with the typical values of voltages used for these logic families. [6+5]

8. a) Discuss the factors and their relation responsible for directions of counting by a Ripple Counter.

b) Design a Modulo-10 Ripple counter counting Upwards.

[6+5]

9. a)Show the uses of D-F/F as a T-only F/F; a T-F/F; a JK-F/F.

b) Design a synchronous decade counter counting downwards (1001 to 0000). Use JK-F/F using type-D method of design. Show the Bush-diagram also. [6+5]

10. Write short notes on any two: $[2\times5\frac{1}{2}]$

(a) 5-bit Ring Counter and Johnson Counter;
(b) Simple- and Dynamic-Buffer Registers;
(c) Buffer Register for Common Bus Oriented processor Structure;
(d) Parallel In, Parallel Out, Right Shift and Left Shift , Shift-Registers.