BE (EE) Part-III 5th Semester Final Examination 2012
Subject: Solid State Devices and Circuits -II
(EE 503)

Time: 3 Hours | Full Marks: 70

Use separate answer-script for each half
Answer SIX questions taking THREE from each half
Each question is of equal marks
Two marks are reserved for neatness in each half

FIRST HALF

1. (a) Explain the operation of a transformer-coupled class A amplifier and calculate its maximum possible efficiency. What are the disadvantages of such amplifiers?

   (b) Derive the expressions for voltage gain and input impedance in common drain FET amplifier for high frequency operation.

   [(2+3+2) + (3+1)]

2. (a) Describe the high frequency model of a BJT and derive the expression for higher cut-off frequency of a common-emitter amplifier with resistive load.

   (b) Explain different types of normal over-current protection schemes of a series type voltage regulator.

   [(3+3) + 5]

3. (a) With necessary circuit diagrams and waveforms, explain the operation of a single phase full-wave bridge rectifier. Calculate the rectification efficiency and transformer utilization factor.

   (b) Explain the operation of a dc-dc boost converter and show that the output voltage is always higher than the input voltage.

   [(2+2+3) + 4]

4. (a) Describe the functional block diagram of 555 timer IC and explain its operation as astable multivibrator. How can you control the high and low durations of an astable circuit independently?

   (b) Design the circuit of a voltage regulator using IC 723 for 20V output from 30 V dc input with a current limit of 100mA.

   [(3+3+2) + 3]

5. Write brief notes on:
   (a) Opto-coupler
   (b) Capacitive filter used in linear power supply
   (c) Current mirror

   [4+4+3]

SECOND HALF

6.(a) What is a Sample-Hold circuit (S/H)? With a practical circuit diagram, describe the operation of a S/H circuit using operational amplifiers (OA) and other necessary components.

(b) Describe the operation of two analog-digital converter (ADC) circuits, one using V-T converter block and other using V-F block. Develop input/output relations of these circuits and find the input/output relations considering all linearised blocks in the schemes. [5+6]

7. (a) Realise a simple 5-bit Johnson Counter using D-Flip-flops but using no external gate in the feedback path of a Right-Shift Shift-Resister and count the number of counting states. Is it possible to realise a Ring Counter with minor change in the above counter but without using any external gate? – If 'yes', draw the circuit and count number of counting states with initial value 00001.

(b) Draw the block diagram of an 8-bit Buffer Register and use it in an architecture of a bus-organised structure for interchanging (swaping) of data between the two registers. Write a program for above operation, i.e. show the arrangement as the steps of instructions in sequence of the binary control words converted in hexadecimal system. [6+5]

8. (a) With the help of a block diagram, discuss the hardware parameters and their interrelations for determining the UP/DOWN counting modes of a Ripple Counter.

(b) Design a Modulo-7 UP Ripple Counter using negative edge triggered JK- flip-flops with all CLEAR (Cl) terminals only. [4+7]

9 (a) Design a synchronous counter to count (2) – (7) – (5) – (6) – (2) using JK- Flip-flops following Type-T design method. Show all the design steps with Truth-table, State diagram, K-maps, Bush diagram and the logic circuit.

(b) What is a 4-bit Serial Adder. Draw block diagram of the scheme using one PISO Accumulator and one PISO Register, and describe the operation of the scheme. [7+4]

10. Write short notes on *any two* : [5 ½ ×2]

(a) ECL OR-NOR circuit for integrated circuits;
(b) Parallel Adder-cum-Subtractor circuit for 2's complement Signed Magnitude Numbers;
(c) Programmable ROM using diode-fuse array;
(d) Field Programmable Gate Array;
(e) Analog/Digital MUX-cum-DMUX using CMOS Bi-lateral switch.