B.E. Part II 4th Semester (E.E) Final Semester Examination April, 2012
Subject: S. S. Devices & Ckts-I (EE404)
Attempt three questions from each half
2 marks reserved for neatness in each half

Full Marks-100 **Time 3Hrs**

First Half

1. **(a) From Ebers-Moll equation, derive the expression for junction voltages V_{CB} and V_{EB} in terms of terminal currents I_C and I_E for a P-N-P bipolar junction transistor.**

(b) Show that the emitter junction volt-ampere characteristic of a transistor in the active region is given by

$$I_E \approx I_S e^{\frac{V_E}{V_T}} \quad \text{where} \quad I_S = -\frac{(-I_{OE})}{(1-\alpha_N \alpha_I)}$$

[5 + 6]

2. **(a) The amplifier shown in Fig. 1 uses a transistor whose h parameters are $h_{fe} = 50$ and $h_{ie} = 1.1k\Omega$. Neglect the effect of other h-parameters. Calculate (i) $A_I \equiv \frac{-I_2}{I_b}$ (ii) $R_i \equiv \frac{V_b}{I_b}$, (iii) $A_i' \equiv \frac{-I_2}{I_1}$ Assume all the capacitors are having infinite capacitance.**

(b) Find the bias stability factor against β variation for a self bias circuit

[7+ 4]

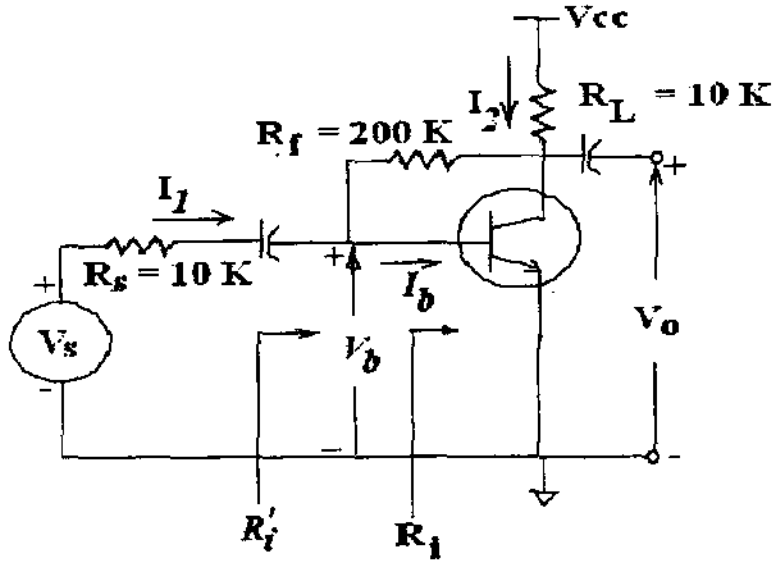

Fig. 1

3. **(a) Show that the trans-conductance g_m of a JFET is related to the drain current I_{DS} by** $g_m = \frac{2}{|V_p|}\sqrt{I_{DSS} I_{DS}}$

(b) Find the voltage amplification $A_v = \frac{V_O}{V_S}$ for the circuit shown in Fig. 2.

(c) The JFET amplifier shown in Fig. 3 has the following parameters: $R_D = 12k\Omega$, $R_G = 1M\Omega$, $R_S = 470\Omega$, $V_{DD} = 30V$, C_s is arbitrarily large, $I_{DSS} = 3mA$, $V_p = -2.4V$, and $r_d >> R_D$. Determine (i) the gate to source bias voltage V_{GS}, (ii) the drain current I_D, (iii) the quiescent voltage V_{DS}, (iv) the small signal voltage gain A_V

[2+4+5]

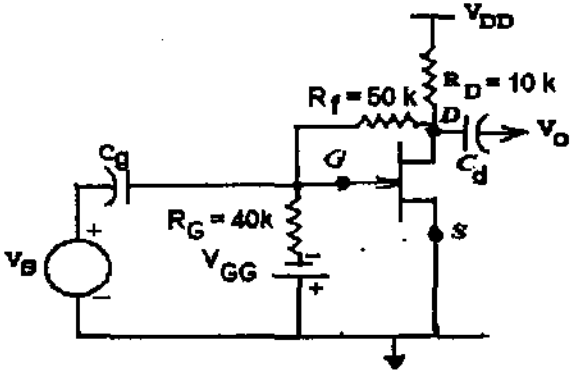

Fig. 2

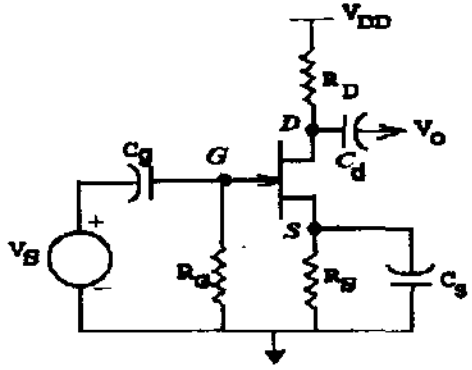

Fig. 3

4. (a) Draw a feedback amplifier in block diagram form and identify each block and state its function., (b) State the three fundamental assumptions which are made in order that the expression $A_f = \frac{A}{1+\beta A}$ be satisfied exactly (c) An emitter follower circuit is shown in Fig. 4. Find the voltage gain of the amplifier using the feedback method of analysis.

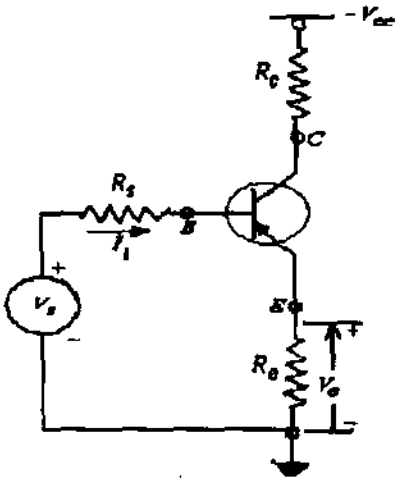

Fig. 4

[2+3+6]

5. Write short notes on any two:- $2 \times 5\frac{1}{2}$

(a) Biasing of JFET and MOSFETs
(b) CMOS structure and its use
(c) Differential gain of a JFET difference amplifier
(d) Advantages of using negative feedback

Second half

6 (a) With the help of circuit diagrams deduce the output expressions, state the advantages and compare a voltage follower circuit and a non-inverting gain amplifier circuit using operational amplifier (OA)

(b) Find out input-output relations of OA based inverting gain amplifier and a two-input adder circuit of gain -10 using 10KΩ. and 100KΩ resistors. Now develop a subtractor circuit utilising these circuits and find out the expression of the output and the gain. **[5+6]**

7 (a) With a circuit diagram, discuss an OA based RC integrator. Find out the input-output expression and compare it with a passive RC integrator circuit.

(b) Describe an Analog Comparator circuit using OA and draw the Transfer Characteristic curve Is it called a ZCD? – Justify. **[5+6]**

8 (a) Realise an XOR gate using not more than four NAND gates. Here the designer is not permitted to use a NOT circuit.

(b) Define a Half Adder (HA) and a Full Adder (FA) circuits. Explain the working of these circuits using Truth Tables, Venn Diagrams, K-Maps and Boolean Algebraic expressions using min-term expressions and Max-term expressions. Realise a HA circuit using a FA circui tand FA using two HA's and an OR gate. What happens when The OR gate is replaced by aan XOR gate. **[5+6]**

9 (a) Using the truth table method show that Y1 = Y2, where
Y1 = A B' + B C' + A' C and Y2 = A' B + B' C + A C'
And also realise both the expressions using AND-OR circuits.

(b) Minimise the following POS function (Y3) analytically and also using QMC tabular method including Prime Implicant table for optimised relation

$$Y3 = \prod M (1, 2, 3, 4, 8, 12)$$

Realise the Boolean system, Y3, with NAND-NAND combination. **[5+6]**

10 (a) Using XOR gates and other suitable gate, draw the 4-bit Word Comparator circuit and obtain the Truth Table and K-Map. Consider that output is HIGH when the two words are EQUAL.

(b) Minimise the following 3-input 2-output digital system in NAND-NAND configuration with not more than six NAND gates

$$Y4 = \prod M (3, 4, 5, 7)$$

$$Y5 = \prod M (2, 5)$$ **[5+6]**
