BENGAL ENGINEERING AND SCIENCE UNIVERSITY, SHIBPUR
B.E.(CST) THIRD SEMESTER FINAL EXAMINATION, 2012
Digital Logic (CS 301)
Answer any five questions.

F.M. 70 Time: 3 hrs

1 a) Find the complement of the following Boolean expression and reduce it to a minimum number of literals.

$$(B\overline{C} + \overline{A}D)(A\overline{B} + C\overline{D})$$

b) Determine the minimum sum of products and minimum product of sums for:
$f = \overline{b}\,\overline{c}\,\overline{d} + bcd + ac\overline{d} + \overline{a}\,\overline{b}c + \overline{a}b\overline{c}d$

c) What are the major applications of open-collector TTL gates? [5 + 7 + 2]

2 a) Draw the circuit diagram of a two input DTL NAND gate and connect its output to N inputs of other similar gates. Assume that the output transistor is saturated and assume $h_{FE} = 20$.

i Calculate the current coming from each input connected to the gate.

ii Calculate the total collector current in the output transistor as a function of N.

iii What is the fan-out of the gate?

b) Define noise margin and propagation delay of a logic gate. [10 + 4]

3. a) Show that how a full-adder can be converted to full-subtractor with the addition of one inverter circuit.

b) Design a combinational circuit that converts a four-digit binary number to a decimal number in BCD. Note that two decimal digits are needed since the binary numbers range from 0 to 15. [5 + 9]

4. a) A combinational circuit is defined by the following three functions:

$$F_1 = \overline{X}\,\overline{Y} + XY\overline{Z},\ F_2 = \overline{X} + Y \text{ and } F_3 = XY + \overline{X}\,\overline{Y}$$

Design the circuit with a decoder and external gates.

b) Construct a 5 × 32 decoder with four 3 × 8 decoder and a 2 × 4 decoder. Use a block diagram construction. [8 + 6]

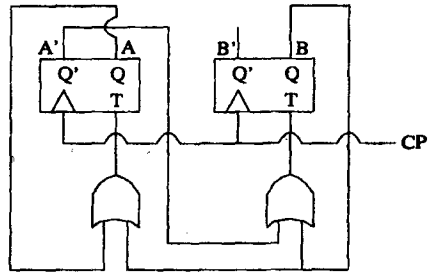

Figure 1:

5. a) Derive the state table and state diagram of the sequential circuit of Figure 1. What is the function of the circuit?

b) Design the sequential circuit described by the following state equations. Use JK flip-flops. [7 + 7]

$$A(t+1) = xAB + y\overline{A}C + xy$$
$$B(t+1) = xAC + \overline{y}B\,\overline{C}$$
$$C(t+1) = \overline{x}B + yA\,\overline{B}$$

6. a)Define combinational circuits and sequential circuits.

b) Design a Mod-5 synchronous counter using J-K flip-flops so that if at any time the unused states 101, 110 and 111 appear, the next clock will reset the counter to 000. [4 + 8]

7. a)Draw the diagram of a 4-bit binary ripple down-counter using JK flip-flops that trigger on the negative-edge transition. Also draw a timing diagram for the same circuit.

b) Design a synchronous BCD counter with JK flip-flop. [6 + 8]

8. Write short notes on the following. [8 + 6]

i) Bidirectional Shift Register with parallel loading

ii) Priority Encoder