B.E. (CST) 4[th] Semester Examination *M o*
Department of Computer Science and Technology
, Bengal Engineering and Science University, Shibpur
Sub: Electronic Design Automation
(CS-404)

Time: 2 hour FM: 35

Answer any two from each group
One mark is reserved for neatness

Group-A

1. (a) Discuss overloaded subprogram and overloaded enumeration with example,
   (b) What is the function of package declaration and package body?
   5+3.5
2. (a) What is function attribute?
   (b) type STATUS is (SILENT,SEND,RECEIVE);
   subtype DELAY-TIME is TIME range 50 ns downto 10 ns;
   Write down the output of the following function attribute:
   (i) DELAY-TIME'PRED(10 ns)
   (ii) DELAY-TIME'SUCC(29 ns)
   (iii) STATUS'SUCC(RECEIVE)
   (iv) STATUS TRED(RECEIVE)
   0.5+2x4
3. Write a VHDL code of modulo 5 up synchronous counter. 8.5

Group-B

4. (a) Discuss procedural continuous assignment with example,
   (b) How it differ from regular procedural assignment?
   8+0.5
5. (a) What is the function of zero delay control type of delay based timing control?
   (b) How level sensitive timing control differs from event based timing control?
   3+5.5
6. Write a verilog code of modulo 5 down synchronous counter. 8.5