B. E. Part II (CST) 4th Semester Examination, 2010

Subject: Computer Organization
Time: 3 hours

Paper: CS-402
Full marks: 70

Answer any 4

l.a) Consider the following reservation table for a 4-stage (S'. S», S', and S«) pipeline:

—> clock cycle

1 2 3 4 5 6

i) Show the pipeline architecture corresponding to the reservation table
ii) Identify the forbidden and non-forbidden latecies
iii) Find out collision vector of the pipeline architecture
iv) Draw the state diagram
v) Indemify simple cycles and greedy cycles
vi) Compute M AL & lower bound of MAL 14

b) Define CPI. Consider the following reservation table for a 4-stage (S', S', S', and S«) instruction pipeline of a CPU:

. . . . > clock cycle

1 2 3 4

Comment on the CPI of the CPU instruction execution. 3.5

2.a) Define 4-way set-associative cache system. Consider a cache (Ml) and memory (M2) hierarchy in a 4-way set-associative cache system, where

M1: 64K words
M2: 1G words

Assuming 32 word cache blocks:

i) show the mapping between M2 & M1
ii) how wide are the tags in this cache?
iii) which memory addresses are mapped to the set number 5in the cache? 10

b) Show the design of a 2k x 16 RAM module with four lk x 8 memory modules. 7.5

3.a) State Booth's algorithm for multiplication of two 2's complement numbers. Show the execution steps of Booth's algorithm for the multiplicand Y=1010 and multiplier X=0101. where both the X & Y are represented in 2's complement. 12

b) Explain how data transfer between I/O device and CPU is done in interleaved DMA. 5.5

4.a) Describe in brief the data dependent opcode optimization scheme. 6
b) Explain in brief the relative addressing of operands. 4
c) What is CAM? Find out the expression of match logic of a CAM. 7.5

5. Write micro-programs to emaluate the single-address instructions LOAD X, STORE X. AND X and JUMP X. Briefly describe the design steps of a hardwired control unit, following sequence counter method, for a m/c with these instructions in its instruction set. 17.5

6. a) Indicate the basic features of a ERCW shared memory SIMD ni/c. Describe the method of broadcasting a message in such a SIMD m/c. 12

b) Describe the basic principles of instruction execution in a superscalar processor with issue rale m=3 and Iatency=l. 5.5

7. Write short notes on the following:
a) Memory interfacing with complete decoding 10