BENGAL ENGINEERING AND SCIENCE UNIVERSITY, SHIBPUR
B.E.(CST) THIRD SEMESTER FINAL EXAMINATION, 2011
Digital Logic (CS 301)
Answer any five questions.

F.M. 70 Time: 3 hrs

1 a) Express the following function in a sum of minterms and a product ~~of maxterms.~~

$$F(w,x,y,z) = \overline{y}z + wx\overline{y} + wx\overline{z} + \overline{w}\,\overline{x}z$$

b) Simplify the following Boolean function

$$F(w,\ x,\ y,\ z) = \Sigma(4,\ 5,\ 7,\ 12,\ 14,\ 15) + d(3,8,10).$$

c) Why wired-logic connection is not allowed with totem-pole (TTL) output circuits? [7 + 5 + 2]

2 a) Draw the logic diagram of a two input XOR gate using minimum number of NAND gates.
b) Realize a full adder circuit using TTL-open collector IC (74156) decoder and one inverter.
c) Show how a full adder can be made to subtract. [3 + 6 + 5]

3 a) Construct truth table and write the Boolean expressions for the following verbal problem statement: Two motors, M_1 and M_2, are controlled by three sensors, S_1, S_2, and S_3. One motor, M_2, is to run whenever all three sensors are ON. The other motor is to run whenever sensors S_2 or S_1, but not both are ON and S_3 is OFF. For all sensor combinations where M_1 is ON, M_2 is to be OFF, except when all three sensors are OFF the both motors must remain OFF.
b) Realize the following Boolean function using the appropriate multiplexer.

$$F(A,\ B,\ C,\ D) = \Sigma(1,\ 4,\ 5,\ 7,\ 8,\ 12,\ 13,\ 15)$$

[8 + 6]

4 Design a combinational logic circuit that will convert a straight BCD digit to an excess-3 BCD digit. (i) Construct the truth table, (ii) simplify each output function and write the reduced logic equations, and (iii) draw the resultant logic diagram. [5 + 5 + 4]

5 a) A full-adder receives two external inputs X and Y; the third input Z comes from the output of a D flip-flop. The carry output is transferred to the flip-flop in every clock pulse. The external output S gives the sum of X, Y and Z. Obtain the state table and state diagram of the sequential circuit.
b) Design a sequential circuit with JK flip-flops to satisfy the following state equations:
$A(t+1) = \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C + ACD + A\overline{C}\,\overline{D}$
$B(t+1) = \overline{A}C + C\overline{D} + \overline{A}B\overline{C}$
$C(t+1) = B$ [7 + 7]

6. a) Design a 3-bit counter using D-flip-flops such that not more than one flip-flop changes state between any two consecutive states.

b) Design a Mod-5 synchronous counter using J-K flip-flops so that if at any time the unused states 101, 110 and 111 appear, the next clock will reset the counter to 000. [6 + 8]

7. a) Why we do not use S = 1 and R = 1 as an input sequence in case of R-S (using NOR gates) flip-flop? What is the problem in J-K flip-flop and how is it removed?

b) A Serial adder of Fig. 1 uses two 4-bit shift registers. Register A holds the binary number 0101 and register B holds 0111. The carry flip-flop Q is initially cleared. List the binary values in register A and flip-flop Q after each shift.

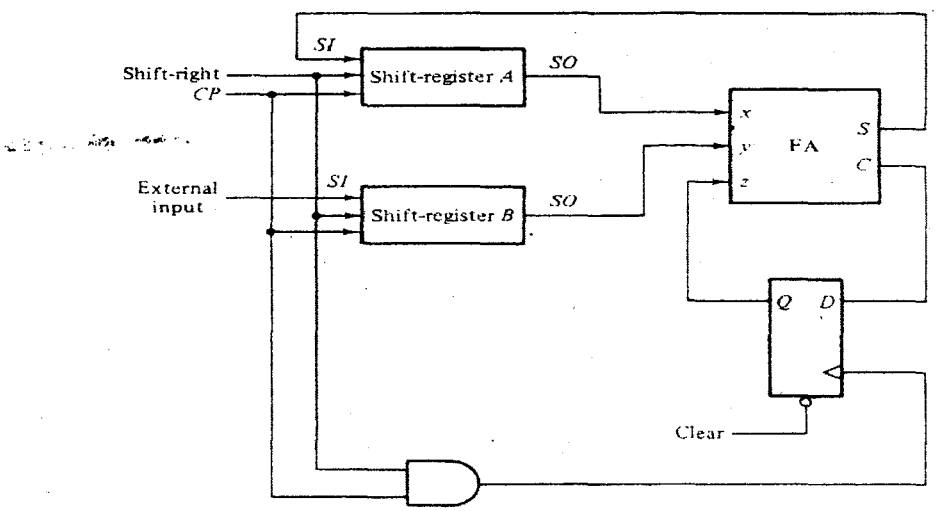

Figure 1:

c) Define the terms (i) fan-out, and noise margin. [4 + 6 + 4]

8. Write short notes on the following. [8 + 6]

i) Tri-state TTL inverter

ii) Johnson counter