Time - 3 hours   Full marks - 100

Answer any five questions.

1. a) Draw the electrical characteristics of CMOS inverter indicating the different zones of operation of the transistor with relevant current - voltage equations. Comment on the relationship between β_n/β_p ratio and inverter characteristics.

b) What is the functional difference between enhancement mode and depletion mode devices?

$$[(13 + 3) + 4]$$

2. a) Draw the CMOS logic diagram of an one bit shift register cell and draw the stick layout for the same. Why two phase clock signals are used in above circuit?

b) Compare the two scaling methods, namely, (i) the constant field scaling and (ii) constant voltage scaling. $[(10 + 2) + 8]$

3. a) Compare the relative merits of three different forms of pull-up for an inverter circuit. What is the best choice for realisation in NMOS technology?

b) Draw the logic diagram of a BICMOS inverter circuit and explain its operation.
c) Compare pass transistor and transmission gate. $[8 + 8 + 4]$

4. a) Define the following terms:
(i) standard unit of capacitance and
(ii) fundamental time constant.
b) A layer of MOS circuit has a resistivity $\rho = 1$ ohm cm. A section of this layer is 55 μm long and 5 μm wide and has a thickness of 1 μm. Calculate the resistance from one end of this section to the other(along the length). Use the concept of sheet resistance R_s. What is the value of R_s?

c) Derive expression for the delay of CMOS inverter circuit. $[4 + 6 + 10]$

5. a) What are the different layout styles in VLSI design? Which one is preferable for Micro-processor design and why?

b) What are the merits and limitations of PLA layout?

c) What are the advantages and disadvantages of standard-cell layout compared to gate-array layout?

d) What are the drawbacks of Kernighan-Lin algorithm in respect of partitioning?
$$[5 + 6 + 5 + 4]$$

6. a) Implement the Boolean function $Z = \overline{(D + E + A)(B + C)}$ using CMOS technology. Assume that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors. Calculate the equivalent (W/L) ratios of the nMOS network and pMOS network.

b) Design a circuit to implement logic function F, use an AOI (AND-OR-INVERT) gate. Draw a transistor-level schematic using CMOS technology. [12 + 8]
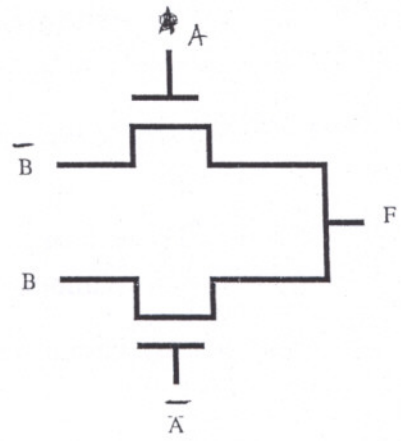
7 a) Draw the circuit diagram of a six transistor static memory cell. Explain its read and write operations with necessary circuit diagrams.

b) How do you apply Lee's algorithm for interconnection of multi-pin nets? Describe the procedure. [12 + 8]

8. Write Short notes on: [6 + 6 + 8]
i) Parasitic effect in CMOS inverters.
ii) Super buffers.
iii) Dynamic Read-Write Memories.