M.E. (ICE), Part-I First Semester Examination, 2011

Advanced Computer Architecture
(ICE-905/4)

Full Marks : 70 Time : 3 hours

Answer any 7 questions

1. i) Write MIPS code for Nested loops
   ii) How do you load larger constants?
   iii) What are the differences between base addressing and PC-relative addressing mode? 3+3+4

2. a) How do you define Performance?
   b) Compare performances of A and B machine. A runs a program in 20 seconds and machine B runs the same program in 25 seconds.
   c) Consider to different implementations, P1 and P2 of the same instruction set. There five classes of Instructions (A, B, C, D and E) in the instruction set. P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is as follows:

Class	:	A	B	C	D	E
CPI on P1	:	1	2	3	4	3
CPI on P2	:	2	2	2	4	4

   Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence.
   i) What are the peak performances of P1 and P2 expressed in instructions per sec.?
   ii) if the number of instructions executed in a certain program is divided equally among the classes of instructions, except for class A, Which occurs twice as often as each of the others, how much faster is P2 than P1?
   1+1+(4+4)

3. a) What is Amdahl's Law?
   b) A program runs in 100 seconds on a machine, with multiply responsible for 80%. How much do we have to improve the speed of multiplication if we want the program to run 4 times faster? How about making it 5 times faster?
   c) Suppose we enhance a machine making all floating-point instructions run five times faster. If the execution time of some benchmark before the floating-point enhancement is 10 seconds, what will the speedup be if half of the 10 seconds is spent executing floating-point instructions?
   d) Suppose we wish to run a program P with $7.5X10^9$ instructions on a 5GHz machine with a CPI of 0.8. What is the expected CPU time?
   2+(2+2)+2+2

4. a) How do you speed up the adder circuit in MIPS ALU using a 16-bit CLA adder with 2 levels of look ahead?
   b) How do you implement the Sequential shift add multiplier?
   c) Write range of values for unsigned and signed multiplication. 6+3+1

5. a) What are the problems with single cycle design?
   b) Write a table for different control inputs for Single cycle MIPS.
   c) Draw the block diagram implementation for Multi-cycle approach. 3+3+4

6. a) What are the five steps of each instruction in multi-cycle implantation?
   b) Calculate the delay for the instructions {add, sub, and, or, slt, sw, lw, beq, j}.
   b) How do you calculate the clock period for multi-cycle design? 3+4+3

7. a) How is the resource utilized in single cycle design, multi-cycle design, pipeline design?
   b) Draw cycle time and CPI for different implementations.
   c) Draw the abstract model of pipelined data path.
   3+3+4

8. (a) What are different types of parallelism?
   (b) Write the Flynn's classification of Parallelism?
   (c) Explain two classifications with the help of schematic diagrams. 2+2+6

9. a) A CPU needs 50 ns for instruction fetch. Calculate performance improvement if instruction prefetch feature is included in the processor. Assume that 20% of the instructions are branch instructions.
   b) A CPU has 1KB memory space. Design a four-way memory interleaving with memory ICs of 50ns cycle time and calculate the effective bandwidth. 5+5

10. a) State the difference between procedure and function with suitable examples in context of VHDL Programming.
    b) Briefly define the problem of Side effect associated with procedures in VHDL.
    c) What are the benefits of using Packages in VHDL – state with suitable example. 4+2+4

11. a) Define Block configuration and Component configuration used in VHDL.
    b) Briefly describe the types of architectures used in VHDL with suitable examples.
    4+6