M.E. 1st SEMESTER (ETC) FINAL EXAMINATIONS, 2013
VLSI Logic Design (ETC-920)

Time: 3 hours Full marks: 70

Answer any **Five** questions **taking at least two from each half**

(Use separate answer script for each half)

FIRST HALF

(1) Write down the CORDIC algorithm for both vectoring and rotation operation. Perform VLSI design for a parallel CORDIC processor for both operations. Explain also the various sub-blocks used in this design. (14)

(2) (a) Explain with the help of flow chart the various steps in VLSI design flow.
(b) Explain with necessary diagrams, the input output blocks of FPGA. (14)

(3) Write down the decimation-in-frequency FFT algorithm. Perform the VLSI design of a serial FFT processor describing necessary sub –blocks. (14)

(4) Write notes on:
(i) 4x4 unsigned binary array multiplier.
(ii) Built in self test in VLSI. (14)

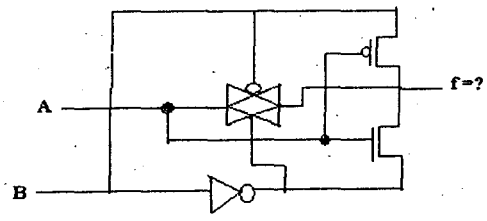
SECOND HALF

(5) a) Discuss the factors on which threshold voltage of MOS transistor depends.
b) Discuss the relative merits and demerits of constant field scaling and constant voltage scaling. (14)

(6) a) Discuss various voltage dependent capacitances of MOSFETs. In which region (s) MOS offers the maximum capacitance and why?
b) Discuss the advantage of transmission gate logic over pass transistor logic. (14)

(7) a) What is the disadvantage of dynamic logic? How that can be circumvented by Domino Logic? Discuss the purpose of weak pull up transistors in Domino CMOS logic
b) Discuss the variation of switching threshold voltage (V_T) of CMOS inverter with transconductance ratio (K_R=Kn/Kp)
(14)

(8) a) Discuss the following i) DIBL ii) Lowly doped drain structure iii) Hot carrier degradation.
b) Discuss the operation of the circuits shown below and find 'f'.



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