Bengal Engineering and Science University, Shibpur
M.E. 1st SEMESTER (ETC) FINAL EXAMINATION, 2012
VLSI Logic Design (ETC-920)

Time: 3 hours Full marks: 70

Answer any **Five** questions **taking at least two from each part**
Use Separate Answer Script for each part

Part 1

(1) Write down the CORDIC algorithm for both vectoring and rotation operation. Perform VLSI design for a parallel CORDIC processor for both operations. Explain also the various sub-blocks used in this design. (14)

(2) (a) Explain with the help of flow chart the various steps in VLSI design flow.
(b) Explain with necessary diagrams, the routing channels of XILINX-FPGA. (14)

(3) Write down the decimation-in-frequency FFT algorithm. Design the address generator block for DIF FFT algorithm describing all the sub-blocks. (14)

(4) Write notes on:
(i) 4 bit loadable up/down binary counter using D flip flops
(ii) 4 bit unsigned parallel divider (14)

Part 2

(5) a) Discuss the factors on which threshold voltage of MOS transistor depends.
b) Discuss the relative merits and demerits of constant field scaling and constant voltage scaling. (14)

(6). a) Plot the variation of different oxide related capacitance as a function of gate voltage for MOSFETs. In which region (s) MOS offers the maximum capacitance and why?
b) Differentiate between short channel and narrow channel effect. (14)

(7). a) Discuss the operation of dynamic logic? What are the problems of these circuits and how that can be circumvented by Domino logic?
b) Discuss the role of weak pull up transistor in minimizing charge leakage of domino logic. (14)

(8). a) Discuss the following i) Substrate Current Induced Body effect ii) Punch through iii) Hot carrier degradation.
b) Implement XOR gate using Complementary Pass Transistor Logic.

(14)