Bengal Engineering and Science University, Shibpur
M.E. 1st SEMESTER (ETC) FINAL EXAMINATION, 2013
Integrated Circuit Technology (ETC-913)

Time: 3 hours Full marks: 70

Use Separate Answer Script for each group
(Answer any two questions from each group)
(One mark in each group is reserved for neatness)

Group A

1. a) Deduce the relationship between doping distribution and fraction solidified for different segregation coefficients.

b) A silicon ingot, which should contain 10^{16} boron atoms/cm^3, is to be grown by the Cz method. What concentration of boron atoms should be in the melt to give the required concentration in the ingot? If the initial load of silicon in the crucible is 60kg, how many grams of boron (atomic weight 10.8) should be added? The density of molten silicon is 2.53 g/cm^3. Segregation coeffieient of boron (k_0) is 0.8. (17)

2. a) A silicon sample is oxidized in dry O_2 at 1200°C for 1 hr. (a) What is the thickness of the oxide grown? (b) How much additional time is required to grow 0.1μm more oxide in wet O_2 at 1200°C.(Rate constant for dry O_2 at 1200°C , A=0.04 μm and B=0.045 $\mu m^2/h$, τ=0.027h, Rate constant for wet O_2 at 1200°C , A=0.05 μm and B=0.72 $\mu m^2/h$)

b) What is the significance of the term i) linear arte constant and ii) parabolic rate constant. (17)

3. a) Discuss the difference between positive and negative photoresist.

b) Discuss the chemical vapor deposition process of silicon. (17)

4. a) For a boron diffusion in silicon at 1000°C, the surface concentration is maintained at 10^{19} cm^{-3} and the diffusion time is 1 hour. Find Q(t) and the gradient at x=0 and at a location where the dopant concentration reaches 10^{15} cm^{-3}. The diffusion coefficient of boron at 1000°C is $2x10^{14}$ cm^2/s.

b) Discuss the significance of the term i) projected range (R_p) ii) projected straggle (σ_p) and iii) lateral straggle ($\sigma_\perp$) with reference to ion implantation process. (17)

Group B

5a) What are homo and hetero epitaxy? Mention the defects introduced at the interface due to epitaxy? Give an example of a device where epitaxy is essential.

b) Why an optimum vacuum is required for the thermal evaporation of metal on silicon substrate? What factors determine the spacing between the target and source in the process?

c) What is electromigration process? To avoid electromigration problems the maximum allowed current density in an aluminum runner is about $10^5 A/cm^2$. If the runner is 3mm

long, 2μm wide and nominally 1μm thick and if 30% of the runner length passes over steps and is only 0.5μm thick there, find the total resistance of the runner if the resistivity is $2x10^{-6}\Omega$-cm. Find the maximum voltage that can be applied across the runner.

d) Why multilevel metallization is required in VLSI? Discuss briefly the process of fabrication with multilevel metallization

(5+3+4+5)

6a) In ion implantation process, the maximum concentration of the implanted ions is within the substrate and not at the surface unlike thermal diffusion and also its lateral straggle is less than that of diffusion process. Why?

b) If a 50keV boron ion is implanted into the silicon substrate, calculate the damage density. Assume silicon atom density is $5.02x10^{22}$atomscc, the silicon displacement energy is 15eV, the range is 2.5nm and the spacing between silicon lattice planes is 0.25nm, projected range is 0.18μm and the energy loss is 60eV/nm.

c) A silicon pn junction is formed by implanting boron ions at 80keV through a window in an oxide. If the boron dose is $2x10^{15}$ cm^{-2} and the n-type substrate concentration is $10^{15}cm^{-3}$, find the location of the metallurgical junction (R_p=0.3μm and σ_p=0.06 μm)

d) Mention two techniques for obtaining good step coverage during metallization by physical vapor deposition.

e) Why a rapid thermal annealing process reduces the damage caused to the crystal lattice without increasing the straggle of ion implantation?

(4+4+3+2+4)

7a) Show the process flow for fabrication of a p-n junction diode of lateral dimensions 100μm by 50μm on a p-type substrate separated by 500 μm from a diffused n+ resistor of dimensions 200 μm by 20 μm on the same substrate. Draw the top view of the masks with dimensions indicated at every stage.

b) Show the process flowchart for the fabrication of two nMOS transistors on a n-type substrate.

(9+8)

8a)What is meant by bulk and surface micromachining? Mention their relative advantages and disadvantages.

b) Discuss the process flow for fabrication of a cantilever beam of 100 μm length, 10 μm width and 2 μm thick.

c) Discuss the process steps for fabrication of a bipolar junction transistor with a collector resistor whose doping concentration is larger than the substrate and the epitaxial layer.

(3+7+7)