Bengal Engineering and Science University, Shibpur
M.E. 1st SEMESTER (ETC) FINAL EXAMINATION, 2012
Integrated Circuit Technology (ETC-913)

Time: 3 hours Full marks: 70

Use Separate Answer Script for each group
(Answer any two questions from each group)
(One mark in each group is reserved for neatness)

Group A

1. a) Discuss with schematic diagram, the 'Czochralski' technique for crystal growth of silicon. Discuss the relative merits and demerits of this process compared to 'Float Zone' process.
   b) Deduce the relationship between doping distribution and fraction solidified for different segregation coefficients. (17)

2. a) A silicon sample is oxidized in dry O_2 at 1200°C for 1 hr. (a) What is the thickness of the oxide grown? (b) How much additional time is required to grow 0.1μm more oxide in wet O_2 at 1200°C.(Rate constant for dry O_2 at 1200°C , A=0.04 μm and B=0.045 $\mu m^2/h$, τ=0.027h, Rate constant for wet O_2 at 1200°C , A=0.05 μm and B=0.72 $\mu m^2/h$)
   b) Discuss the various methods for oxide thickness measurements. (17)

3. a) Discuss the pattern transfer technique using positive photoresist.
   b) Discuss various types of crystal defects in semiconductors. (17)

4.. a) For a boron diffusion in silicon at 1000°C, the surface concentration is maintained at 10^{19} cm^{-3} and the diffusion time is 1 hour. Find Q(t) and the gradient at x=0 and at a location where the dopant concentration reaches 10^{15} cm^{-3}. The diffusion coefficient of boron at 1000°C is $2x10^{14}$ cm^2/s.
   b) Discuss the significance of the term i) projected range (R_p) ii) projected straggle (σ_p) and iii) lateral straggle ($\sigma_\perp$) with reference to ion implantation process. (17)

Group B

5.a) How is the degree of anisotropicity, selectivity and etch rate uniformity of an etchant defined?
b) Explain a mechanism to obtain both selective and isotropic etching.
c) A <100> oriented silicon crystal is etched in a KOH solution through a 5μm by 5μm window defined in silicon dioxide. The etch rate normal to (100) planes is 0.6μm/min. Show the etched profile after 30 seconds and 60 seconds.
d) A silicon wafer is 500 μm thick and it needs to be etched away by 200 μm on the whole. What is the etchant required and explain its mechanism of etching?
(4+5+4+4=17)

6.a) Discuss the process flow for fabrication of a bulk micromachined MEMS piezoresistive pressure sensor
b) What is the advantage of surface micromachining and discuss the process flow for fabrication of a cantilever beam of 200 μm length, 20 μm width and 5 μm thick.
(9+8=17)

7.a) Discuss the process of epitaxial growth of doped silicon on a silicon substrate. Explain with an example where such step is essential.

b) What are the defects introduced at the interface due to epitaxy and how they affect the device functioning?

c) Why an optimum vacuum is required for the thermal evaporation of metal on silicon substrate? What factors determine the spacing between the target and source in the process?

d) What is electromigration process? To avoid electromigration problems the maximum allowed current density in an aluminium runner is about $5x10^5 A/cm^2$. If the runner is 2mm long, 1μm wide and nominally 1μm thick and if 20% of the runner length passes over steps and is only 0.5μm thick there, find the total resistance of the runner if the resistivity is $3x10^{-6}\Omega$-cm. Find the maximum voltage that can be applied across the runner.

e) What is the use of fabricating 'vias' in ULSI circuits and how they are carried out?

(4+3+3+4+3=17)

8.a) Show the flowchart for fabrication of a npn BJT indicating the measure taken to reduce the base width and the collector resistance.

b) In a MOS transistor which parameters are considered to be circuit design parameters and why? Draw the flowchart for fabrication of a CMOS on a p type substrate.

(10+7=17)