Indian Institute of Engineering Science and Technology, Shibpur

M.E. (ETC) 2nd Semester Final Examination, 2014

Advanced Instrumentation (ETC-1014)

Time: 3 hours Full marks: 70

Answer any five questions

1.a. Design a scheme to measure a wide dynamic range of resistance from 1MΩ to 10kΩ with a resolution of 0.1% in the entire range.

b. Design an instrumentation scheme to measure both the capacitance and resistance of a sensor whose resistance is within 10kΩ to 100kΩ and the frequency independent capacitance is between 10nF to 100nF.

(7+7)

2. Design a portable signal conditioning unit to measure the response of an impedance sensor whose sensitivity varies with frequency. The specifications are:
   - i) Amplitude of applied sine wave:<100mV
   - ii) Frequency of operation—100Hz, 300Hz, 1kHz, 5kHz.
   - iii) Impedance of sensor resistance varies from 1kΩ to 10kΩ
   - iv) Maximum sensitivity has to be displayed on LCD.

(14)

3.a. Why MOS transistors are used in the design of ASIC chips?

b. Obtain the small signal voltage gain for the following:

i) Constant current source load common source MOS amplifier.

ii) Diode connected load common source MOS amplifier

(4+10)

4.a. Draw the circuit of a cascode amplifier and obtain its small signal gain. Explain the origin of the gain.

b. Indicate the various capacitances associated with a MOS transistor and obtain the bandwidth of a common source, common drain and a common gate amplifier.

(7+7)

5.a. Obtain the small signal voltage gain of a double ended differential amplifier.

b. Plot the dc transfer characteristics showing the variation of current and output voltage with input common mode voltage.

(7+7)

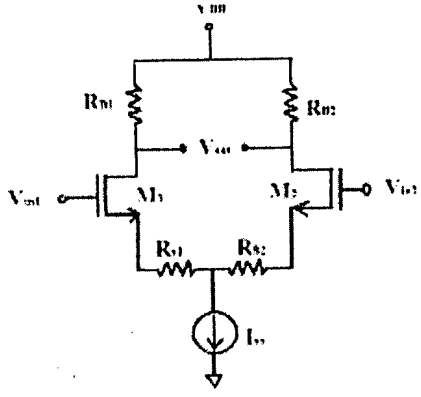
6. What is CMRR? Obtain the expression of CMRR in a double ended differential amplifier if (i) there is a mismatch between the load resistors and (ii) if there is a mismatch in the transconductance values of the MOS transistors.

(14)

7.a. Explain the reason for a high voltage gain in a single ended differential amplifier.
b. Obtain the small signal voltage gain of a single ended differential amplifier.

(7+7)

8. Assuming no symmetry, calculate the small signal voltage gain in Fig.1.



(14)

Fig.1

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