Indian Institute of Engineering Science and Technology, Shibpur
M.E (ETC) 2nd Semester Examination 2014
Switching Theory and VLSI Design (ETC 1013)

Time: 3 hours Full marks: 70

Answer any Five questions **taking at least two from each part**
Use separate answer script for each part

FIRST HALF

(1) Write down the CORDIC algorithm for both vectoring and rotation operation. Perform VLSI design for a serial CORDIC processor for both operations. Explain also the various sub-blocks used in this design. (14)

(2) (a) Explain with the help of flow chart the various steps in VLSI design flow.
(b) Design an additive array multiply module to implement following function
$P=AXB + C + D$
($A=a_3\ a_2\ a_1\ a_0$, $B=b_1\ b_0$, $C= c_3\ c_2\ c_1\ c_0$, $D= d_1\ d_0$) (14)

(3) Perform VLSI design of a serial FFT processor for decimation-in-frequency FFT algorithm. Explain also briefly functionality of various sub-blocs used in the design. (14)

(4) Write notes on:
(i) Built-in-Self-Test for VLSI testing
(ii) 4-bit parallel divider (14)

SECOND HALF

(5) a) Amongst a CMOS NAND and NOR gate which one is better and why?
b) Discuss the voltage transfer characteristics of CMOS inverter with emphasis on region of operation of n-MOS and p-MOS.
c) Discuss the variation of switching threshold voltage (V_T) of CMOS inverter with transconductance ratio (K_R=Kn/Kp) (14)

(6). a) Discuss various capacitances of MOSFETs in different regions of operations. In which region (s) MOS offers the maximum capacitance?
b) Discuss the relative merits and demerits of constant field scaling and constant voltage scaling. (14)

(7). a) What is the disadvantage of dynamic logic? How that can be circumvented by Domino Logic? Discuss the purpose of weak pull up transistors in Domino CMOS logic.
b) Discuss the operation of CMOS based edge triggered D flip-flop. (14)

(8). a) Discuss various short geometry effects and their consequences of MOS transistors.
b) Discuss the operation of CMOS based XOR gate using 6 transistors. (14)