Bengal Engineering and Science University, Shibpur
M.E. 2nd SEMESTER (ETC) FINAL EXAMINATION, 2013
Switching Theory and VLSI Design
(ETC-1013)

Time-3hours **Full marks-70**

(Use separate answer script for each group)

Group A

(Answer question number **1** and any **Two** from the rest)

1.Design a 16 bit Fractional Multiplier block having relationship $D_{out}=0.707\ D_{in}$, both by serial processing and parallel processing with pipelining. 11

2. What are the differences between FPGA and ASIC? Draw and explain CLB of XLINX SPARTAN FPGA. 12

3.Write down the CORDIC algorithm. Perform VLSI design of a serial CORDIC processor. 12

4. Write notes on
i) Built in self test ii) 4 bit binary parallel divider iii) JK Flip Flop 12

Group B

(Answer question number **5** and any **One** from the rest)

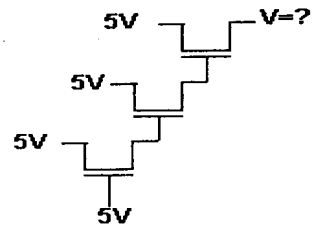
5. Choose the correct alternative(s) (any five) 5 x2=10

a) Threshold voltage (Vt) of MOSFET
i) Increases with increased doping and decreases with decreased oxide thickness
ii) Increases with increased doping and increases with decreased oxide thickness
iii) Decreases with increased doping and decreases with decreased oxide thickness
iv) Decreases with increased doping and increases with decreased oxide thickness

b) Switching Threshold voltage of CMOS inverter
i) Increases ii) Decreases iii) First decreases then increases iv) remain unchanged with increasing transconductance ratio (kn/kp).

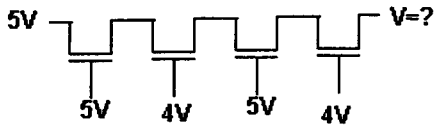
c) For kn=kp , $V_{T,n}=V_{T,p}=1V$, $V_{dd}=5V$, V_{th} (NOR2) and V_{th} (INV) will be
i)2V and 2.5V ii) 2.5V and 2.0V iii) 1V and 2V iv) 2.5V and 2.5V

d) Assume $V_T=1V$



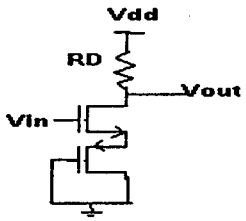
i)2V ii) 1V iii) 3V iv) 4V

e) Assume V_T=1V



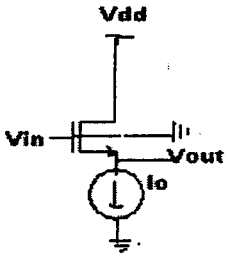
i)2V ii) 1V iii) 3V iv) 4V

f) Assume $\gamma=\lambda=0$,lower transistor is M2, upper one is M1



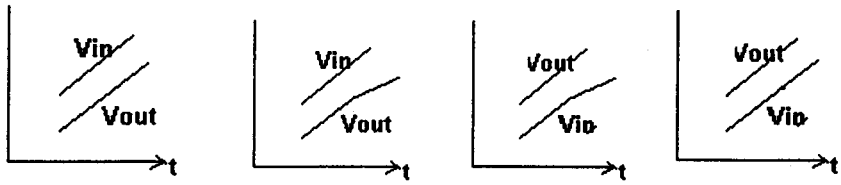
i) $A_v= +R_D/(1/g_{m1}+1/g_{m2})$ ii)$A_v= -R_D/(1/g_{m1}+1/g_{m2})$iii) $A_v= -R_D/(1/g_{m1}+1/g_{ds2})$
iv) $A_v= -R_D/(1/g_{ds1}+1/g_{m2})$

g)



For body bias effect input and output voltage relation is like

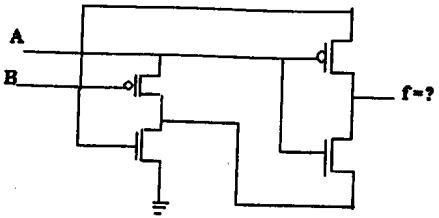
i) ii) iii) iv)



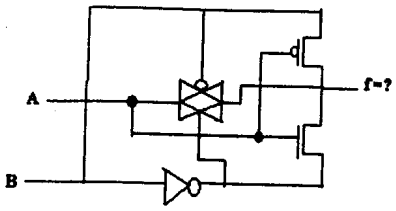
6. (a) Discuss various short geometry effects in MOSFETs.
   (b) What is LDD? Why this is used?
   (c) Deduce the expression of switching threshold voltage of CMOS NAND (2) gate ?
   (d) Discuss the variation of switching threshold voltage (V_T) of CMOS inverter with transconductance ratio (K_R=Kn/Kp) 8+5+7+5=25

7.(a) Discuss the operation of the circuits shown below and find 'f'.

i)



ii)



(c) Discuss the relative merits and demerits of constant field scaling and constant voltage scaling.

(b) What is dual rail CMOS circuit? What is the advantage of such circuit?

(c) Discuss the purpose of weak pull up transistors in Domino CMOS logic.

6+7+6++6=25