Indian Institute of Engineering Science and Technology, Shibpur
M.E (ETC) 2nd Semester Examination 2014
Fault Diagnosis in Digital Systems
(ETC-1012)

Time: 3hours **Full marks-70**

(Use separate Answer Script for each part)

Part-A

(Answer any three from the following)
(In this part 2 marks are reserved for neatness)

1. (a) What is logical fault? Explain how this fault can be detected by simple truth table verification method.
   (b) Describe the one dimensional path sensitizing technique and mention its limitation. [3+8]

2. (a) How a critical error of one gate can be a sub-critical error for another gate.
   (b) Explain with suitable example the general quadded logic design procedure. [3+8]

3. Using 'Marsh Marching Technique' explain how faults can be detected in a memory location of a semiconductor memory array. [11]

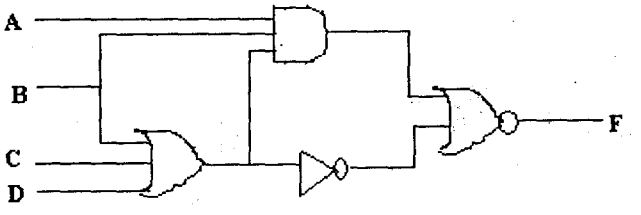
4. (a) Explain digital fault simulation technique and compare it with physical and manual method for simulation.
   (b) Write technical notes on the following:
   (i) Race, (ii) Cycle, (iii) Hazard [5+ (3×2)]

5. (a) Explain how a fault dictionary can be formed? Also mention how the 'fault table' construction method in the detection of fault in a combinational circuit is different from the method of construction of fault dictionary. [6+5]

Part-B

(Answer any **Two** questions)

1. (a) With reference to the Fault diagnosis, what is 'Controllability' and 'Observability' of a system.
   (b) Discuss whether the system shown below is 'fully testable' or not?



17.5

2. (a) What do you understand by the term i) fault coverage ii) fault detection efficiency
   (b) Briefly describe i) stuck on ii) stuck off faults iii) bridging fault. 17.5

3. (a) What do you understand by the nonlinearity problem of switched capacitor circuits?
   (b) How the nonlinearity problem of switch capacitor circuits can be circumvented? 17.5

4. (a) Why should one avoid 'delay dependent logic' while designing digital systems?
   (b) What is redundant logic?
   (c) Briefly discuss 'Mixed D Full Scan Design'. 17.5