Bengal Engineering and Science University, Shibpur
M.E. 2nd SEMESTER (ETC) FINAL EXAMINATION, 2013
Fault Diagnosis in Digital Systems
(ETC-1012)

Time-3hours **Full marks-70**

Part-A

(Answer any three questions from the following
Two marks are reserved for neatness in this half)

1. (a) With suitable example explain what do you mean by the term stuck at '0' and stuck '1' in a digital circuit.
   (b) Explain the 'fault table' construction method in the detection of fault in a combinational circuit. [3+8]

2. (a) Describe the one dimensional path sensitizing technique and mention its limitation.
   (b) How a critical error of one gate can be a sub-critical error for another gate. [8+3]

3. With the help of a flow chart, explain the method of troubleshooting semiconductor memories. [11]

4. (a) With suitable example explain the term:
   (i) Race, (ii) Cycle, (iii) Hazard
   (b) Make a comparison between digital, physical and manual fault simulation technique. [(3×2)+5]

5. (a) With a suitable example explain the general quadded logic design procedure.
   (b) Explain how a fault dictionary can be formed? [6+5]

Part-B

(Answer any two questions from the following)

6. (a) What do you understand by the term i) fault coverage ii) fault detection efficiency
   (b) Briefly describe i) stuck on ii) stuck off faults iii) bridging fault. 17.5

7. (a) With reference to the Fault diagnosis, what is 'Controllability', 'Observability' and 'full testability' of a system. 17.5

8. (a) Why should one avoid 'delay dependent logic' while designing digital systems?
   (b) What is redundant logic?
   (c) Briefly discuss 'Mixed D Full scan Design'. 17.5

9. (a) What is parallel gate evaluation?
   (b) How the nonlinearity problem of switch capacitor circuits can be circumvented? 17.5