M.E. (ETC) 2nd Semester Examination, 2014

Subject: Architecture of Microprocessor & Microcomputer (ETC 1011)

Full marks: 70 **Time : 3hrs**

Answer Q1. any four from the rest questions

Answer should be brief and to the point.
Unnecessary lengthy answer leads to deduction of marks

1. Answer all questions (10)

i) BHE of 8086 microprocessor signal is used to interface the
a) Even bank memory b) Odd bank memory
c) I/O d) DMA

ii) Access time is faster for
a) DRAM b) SRAM c) ROM

iii) On-chip cache has
(a) lower access time than RAM (b) larger capacity than off chip cache
(c) its own data bus (d) become obsolete

iv) CPU performance may be measured in
(a) BPS (b) MIPS (c) MHz (d) VLSI

v) Pipelining improves CPU performance due to
(a) reduced memory access time (b) increased clock speed
(c) the introduction of parallelism (d) additional functional units

vi) RISC machines typically
(a) have high capacity on-chip cache memories
(b) have fewer registers than CISC machines
(c) are less reliable than CISC machines
(d) typically execute 1 instruction per clock cycle.

vii) Branch prediction is used in the context of
(a) pipelining (b) program loops (c) cache memory (d) ALU operation

viii)) In general, pipelining improves which one of the following?
(a) Instruction latency (b) Instruction throughput (c) Instruction count

ix) Which of the following is NOT involved in a memory write operation:
(a) MAR, (b) PC, (c) MDR, (d) Data Bus

x) Which is the fastest storage unit in a usual memory hierarchy?
a) Cache b) Main memory c) Hard disk d) Register

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2. a) An A/D Converter (ADC) have eight analog inputs(IN0 - IN7), 3-bit analog input selection ($A_0A_1A_2$), input Address Latch Enable (ALE), start conversion(SC), CLK, End of Conversion(EOC), output enable(OE), 8-bit latched data outputs(D0-D7) and Start conversion(SC). Interface the ADC to an 8085 microprocessor system having two analogue inputs from temperature and pressure transducers. Store the digital data in two different blocks starting address TEMPDATA and PRESDATA. Develop a suitable circuit diagram. (9)
   b) Write an assembly language program for conversion and transfer the data to above mentioned memory location in the developed system. Assume necessary memory is available in the system. (6)

3. a) What is the difference between microprocessors and microcontrollers?
   b) Describe organisation of 8051 mentioning program memory and Internal & external data memory. What is special function registers (SFR) in 8085? (2+8+5)

4. Draw and explain how different functional blocks are connected in a multi bus organization of a CPU. Write step action for any typical instruction for above mentioned CPU. (15)

5. Consider three different instructions {e.g. Add R1, R2,R4} for a 32 bit μprocessor. Add R1, R2, R4 which represents [R4] = [R1] + [R2] for the single bus μP. Convert three set of step action for the above instructions (15)

6. Generate micro instructions of control unit for a single bus CPU organization. Draw and explain the basic organization of micro programmed control unit to implement above micro instructions. (15)

7. Draw a hardware organization for a pipeline using blocks of a μprocessor. Explain how instructions are pipelined during execution. Why hazard occurs which may occur in instruction pipelined μprocessor architecture and explain them. (15)

8. With neat sketch explain the architecture of an MSP430 microcontroller. Describe how many stages are there in MSP430 Instruction Cycle. (15)