M.E. (ETC) 2nd Semester Examination, 2012

Subject: Architecture of Microprocessor & Microcomputer (ETC 1011)

Full marks: 70 **Time : 3hrs**

The questions are of equal marks
Answer Question No 8 and any four from rest
Answer should be brief and to the point.

1. Interface a 7x5 dot matrix LED using 8255 PPI to a μprocessor. Write an assembly language programming.

2. Draw and explain how different functional blocks are connected in a multi bus organization of a DPU. Write step action for any typical instruction for above mentioned DPU.

3. Consider three different instructions {e.g. Add R1, R2,R4} for a 32 bit μprocessor. Convert three set of step action for the above instructions.

4. Generate micro instructions of control unit for a single bus datapath organization. Draw and explain the basic organization of micro programmed control unit to implement above micro instructions.

5. Draw the register structure of IA-32 and ARM processor. Explain the differences between the two processors.

6. Draw a hardware organization for a pipeline using blocks of a μprocessor. Explain how instructions are pipelined during operation. What are hazards may occur in instruction pipelined μprocessor architecture. Explain any two hazards.

7. What is meant by virtual memory? Discuss virtual Memory Management scheme. Compare any two page replacement policies.

8. i) BHE of 8086 microprocessor signal is used to interface the
   a) Even bank memory b) Odd bank memory
   c) I/O d) DMA

   ii) 8088 microprocessor differs with 8086 microprocessor in
   a) Data width on the output b) Address capability
   c) Support of coprocessor d) Support of MAX / MIN mode

iii) Can ROM be used as stack?
a) Yes b) No c) sometimes yes, sometimes no

iv) The Pentium processor is
a) 16-bit b) 32-bit c) 64 bit d) 8-bit

v) The call instruction modifies
a) the flags register b) program counter
c) bp register d) none of the previous

vi) Access time is faster
a) DRAM b) SRAM c) ROM

vii) A 32-bit **address bus** allows access to a memory of capacity
(a) 64 Mb (b) 16 Mb (c) 1Gb (d) 4 Gb

viii) On-chip cache has
(a) lower access time than RAM (b) larger capacity than off chip cache
(c) its own data bus (d) become obsolete

ix) Which is the fastest storage unit in a usual memory hierarchy?
a) Cache b) Main memory c) Hard disk d) Register

x) Pipelining improves CPU performance due to
(a) reduced memory access time (b) increased clock speed
(c) the introduction of parallelism (d) additional functional units

xi) RISC machines typically
(a) have high capacity on-chip cache memories
(b) have fewer registers than CISC machines
(c) are less reliable than CISC machines
(d) typically execute 1 instruction per clock cycle.

xii) Timesharing is the same as
(a) multitasking (b) multiprogramming (c) multiuser (d) none of the previous

xiii) Branch prediction is used in the context of
(a) pipelining (b) program loops (c) cache memory (d) ALU operation

xiv) In general, pipelining improves which one of the following?
(a) Instruction latency (b) Instruction throughput (c) Instruction count