## BENGAL ENGINEERING AND SCIENCE UNIVERSITY, SHIBPUR M.E. 1<sup>ST</sup> SEMESTER (EE) FINAL EXAMINATION, 2012

Microprocessors, Micro-controllers And their Applications (EE 918)

Time: 3 hours Full Marks: 70

- (i) The questions are of equal value
- (ii) Answer any five questions taking at least two from each group

	Group A	
1.		? What are the $[3 + 1 + 2 = 6]$
	b) What are the functions of $\overline{BERR}$ and $\overline{HALT}$ in M68000? Explain what happens when (i) $\overline{BERR}$ input is received.	ved alone and
	(ii) $\overrightarrow{BERR}$ is received along with $\overrightarrow{HALT}$ .	[1+1+1=3]
	c) What is the outcome of each of the following instructions:	
	<ul> <li>MOVE M.W A5/D1/D3, \$003000</li> </ul>	
	• EXG A2,A4	
	• ASL.W #4, D2	
	• BCHG.B #2, \$002000	
	BEQ *+\$20 Assume any initial content of the registers.	[5]
	Assume any little content of the registers.	[5]
2.	a) Write a 68000 assembly language program to realize the following high-level language program segment:	
	SUM = 0	
	FOR I = 1 TO 10	
	SUM = SUM + A(I) $END EOR$	
	END FOR	
	Assume A to be an array of 16 bit integers and SUM to be a 32 bit integer.	[4]
	b) When an Interrupt Request arrives at one of the inputs of a PIC 8259A, how are the registers IRR, IMR and IS specify the function of each register.	R used? Clearl [4]
	c) What is meant by 'specific rotation' in relation to 8259A? Explain with an example.	[2]
	•	
	d) What is the maximum number of interrupts that can be handled by an 8259A? With a simple block diagram, sl slave configuration of two 8259 PICs indicating clearly all relevant signals.	now the master [4]
3.	a) How is Intel 8251 configured when the mode word is 73H and the command word is 36H is asynchronous mode	? [4]
	b) What is the functional difference between 'TXRDY' and 'TXEMPTY' signals in Intel 8251A?	[2]
	c) What is the function of the SYNDET/BRKDET signal of Intel 8251A in asynchronous transmission?	[2]
	d) Why is USB fast replacing all other bus standards?	[3]
	e) Explain the function of the following signals:	

iii)  $C/\overline{D}$ 

[3]

ii) *INTA* 

DTACK

i)

## Group B

4.a) Explain the multitasking achieved in processors like 80286 and upwards, with reference to the "onionskin" organisation of the memory. [6] What precautions are to be taken foe working in a multi-taking environment? [2] **b**) c) Write a program in ALL for the 8086 microprocessor to move a string of data having N bytes residing at memory location M1 to be shifted to M2. Use specific instructions for this purpose. [6] 5a) Draw the block diagram of the 8051 microcontroller. [5] b)Specify the type of architecture this microcontroller has and its contrast with respect to the ADSP 2101 microcontroller. [4] c) Write a program to take in the data from Port 1 of the 8051 microcontroller and output it through port2 [5] 6a) Draw the base architecture of the ADSP 2101. [5] b) Which part of the DSP is most suited to carry out the digital filtering techniques. Explain with suitable reason. [4] c) Write a program to logically AND two data. One coming from Port1 and the other data stored in memory location M1. Display the output from Port2. [5] 7 a) Write a program in the ADSP 2101 ALL to compute the following sum  $S = 1^2 + 2^2 + 3^2 + \dots$  for N nos. Draw a flowchart for the above computation. **[10]** b) What do you mean by the term 'effective address" in 8086? How is this address generated? [4] 8) Write short note on (any two) [7x2] a) The Prom Decoder chip and its applications.

b) The PLA and PAL configurations and their applications.c) The formation of virtual memory with descriptor table.