M.E. (Electrical)
1st Semester Supplementary Examination, April/May 2013

Subject : Power Electronics I

Code No. **EE 906**

Branch: EE
Time : 3 hours

Full Marks : 70

(i) The questions are of equal value
(ii) Answer any ***three*** questions taking ***only one*** from each group
(iii) One mark is reserved for neat and precise answers.

Group A

1. Answer all parts:

   a) Draw the power circuit diagram of a DC-DC boost converter and explain its operation at steady state with the help of significant waveforms of voltages and currents.
   b) Derive the steady state input-output DC current relationship of the above-referred converter under continuous conduction.

[18+5=23]

2. Answer all parts:

   a) With the help of power circuit diagrams and waveforms, explain the operation of a full-bridge DC-DC converter feeding a DC motor load, operating under bipolar pulse width modulation (PWM).

   Derive the steady state input-output DC voltage relationship of the above-referred converter under continuous conduction.

Group B

3 (a) A 3-phase controlled bridge rectifier having a free-wheeling diode on the output side is fed from 415 V, 50 Hz supply. Assuming a continuous and level load current of 50A and a firing angle of $\alpha = 30^\circ$,

(i) draw the output voltage, input side line current (any one), freewheeling diode current and current through any one controlled device.
(ii) determine the fundamental input side power factor
(iii) calculate the rms value of the fundamental current and the THD
(iv) How will the input current waveform look if the load is shunted by a heavy capacitor? Justify your answer.

(b) A 3-phase fully controlled bridge rectifier is fed from a 415 V, 50 Hz supply. The source side inductance per phase is 12 mH. Neglecting source resistance and rectifier device drops, for continuous and level load current of 40A and a firing angle of $\alpha = 30^\circ$.

(i) evaluate the mean output voltage after deriving necessary relations.
(ii) draw the load voltage and the input line current.

(6 + 2+4+2 + 4+5) =23

4. (a) A 3-phase 3-leg inverter is decided to be operated from a 580 V dc bus following a 120^0 conduction logic at 50 Hz for each switching device. After preparing the appropriate switching sequence table against the different electrical angles draw the switching logic wave forms, the output line and phase voltages, the pole voltages (v_{ao} etc.). With appropriate derivations, comment on the harmonics (including their percent content and Hz values) present in the line and phase voltages.
(b) For the above inverter derive expressions and draw space vectors for a conceptual 150^0 conduction case. Draw the corresponding line and pole voltages against time, assuming a star-connected resistive load (with proper numerical values on the axes).

(2+6+6 +3+6) = 23

Group – C

5. (a) What are the salient features in the construction of power Bipolar Junction Transistor? (b) Draw output characteristic of a power BJT and briefly state its distinctive features. (c) What is storage time? (d) Discuss briefly about SOA of a power BJT (e) A Power BJT is used to switch a diode clamped inductive load carrying 20 A. The supply voltage is 400V dc, switching frequency and duty cycle are 10 kHz and 0.5 respectively. Switching times are as follows. $t_d = 2\mu s$, $t_{ri} = t_{fv1} = 8\ \mu s$, $t_{fv2} = 0$, $t_s = 12\ \mu s$, $t_{fi} = t_{rv2} = 8\ \mu s$, $t_{rv1} = 0$. Calculate switching and conduction losses in the transistor. Justify clearly the assumptions made in the calculation. (f) Explain the operation of MOSFET during drain to source voltage fall time. The MOSFET is used to switch a diode clamped inductive load

[2+3+2+2+7+7]

6. (a) Explain the salient features in the construction of a power MOSFET.
(b) Draw the output v-i characteristic of a power MOSFET and briefly discuss about different zone of operation. (c) Why is it easier to parallel MOSFETs compared to other switching devices? (d) With suitable diagrams, explain the different capacitances formed in a power MOSFET. (e) Explain why latch-up condition can occur in an IGBT, (f) How latch-up can be avoided? (g) An IGBT circuit module complete with its own drive circuit has been made with the following parameter specifications:

$$V_{CEM} = 1000V,\ I_{CM} = 100A,\ \frac{dv_{CE}}{dt} < 1000V/\mu s,$$

$$R_{\theta j-a} = 0.5^oC/W,\ t_{on} = t_{d(on)} + t_{ri} + t_{fv} = 0.3\mu s,$$

$$t_{off} = t_{d(off)} + t_{rv} + t_{fi} = 0.75\mu s,\quad T_{j,\max} = 150^oC$$

This module is to be used in a step down converter circuit with a diode-clamped inductive load. In this circuit the free wheeling diode is ideal, the dc supply voltage is $V_d = 800V$, the load current $I_o = 100A$, and the switching frequency is 20 kHz with a 50% duty cycle. Determine if the IGBT module is overstressed

[2+2+2+2+3+4+8]

M.E. (Electrical) 1st Semester Final Examination, November 2013

Subject: Power Electronics I

Code No. **EE 906**
Branch: EE
Full Marks: 70

Time: 3 hours

(i) The questions are of equal value.
(ii) Answer any ***three*** questions taking one ***from each Group***.
(iii) Use graph paper(s) if required.
(iv) One mark reserved for neat and precise answers.

Group A

1. (a) What are the functions of lightly doped semiconductor layer in a power diode?
(b) Compare NPT and PT structure of power diodes.
(c) Explain how diode turn-on voltage overshoot and turn-off reverse recovery current effect on SOA of switching devices.
(d) Draw the forward bias *v-i* characteristic of power BJT.
(e) Explain emitter current crowding during turn-on and turn-off a power BJT.
(f) A power BJT is used to switch an inductive load with a diode clamp. It is given that $\beta = 10$,

$V_{CE(sat)} = 1.5V$, $R_{\theta_{j-a}} = 1^0 C/W$, $T_{j\max} = 150^o C$, $t_{ri} = t_{fi} = 200ns$,
$t_{fv1} = t_{fv2} = t_{rv1} = t_{rv2} = 50ns$,
and $t_{d(on)} = t_{d(off)} = 100ns$. The BJT is switched at frequency of 20 kHz with 40% duty cycle.
Assuming current to be switched is $I_o = 50A$ and $V_{DC} = 100V$, find (i) the average power dissipated, (ii) temperature rise in the junction of the transistor if ambient temperature is 30° C.

[2+2+3+5+3+(4+4) = 23]

2. (a) Explain from the structure of a power MOSFET that there is an integral diode formed connected between source to drain.
(b) Explain from the structure of an IGBT that there is an integral thyristor structure.
(c) Why source-body is short-circuited with metallic contact in a power MOSFET.
(d) Explain why an IGBT can be conceptualized as a transistor driven by a MOSFET.
(e) Give reason why the current gain β for the transistor section in an IGBT is kept very low.
(f) Explain how the conductivity modulation takes place in drift region of an IGBT.
(g) An n-channel MOSFET is to be used in a step-down converter circuit. The dc voltage V_d = 300V, the load current I_o=10A, the free wheeling diode is ideal, and the MOSFET is driven by a ± 15 V square wave (50% duty cycle and zero dc value) in series with 50 ohm. The MOSFET characteristics are

$$V_{GS(Th)} = 4V, I_D = 10A \; at \; V_{GS} = 7V, C_{gs} = 1000pF,$$
$$C_{gd} = 150pF, r_{DS(on)} = 0.5\Omega$$

Calculate turn-on delay time $t_{d(ON)}$

[2+2+2+2+3+3+9 = 23]

Group B

3. (a) A 3-phase 3-leg inverter is decided to be operated from a 560 V dc bus following a 120° conduction logic at 50 Hz for each switching device. After preparing the appropriate switching sequence table against the different electrical angles, draw with appropriate numerical values, the switching logic wave forms, the output line and phase voltages.
(b) With appropriate derivations, comment on the harmonics (including their percent content and Hz values) present in the line and phase voltages. Find the THD in the output line voltage.
(c) Why can we not have more than 180° and less than 120° conduction in a 3-phase bridge VSI?
(d) For a 3-phase bridge inverter fed from a 560 V DC-link, draw switching logic pulses for a conceptual 150^0 conduction case. Draw the line voltage V_{RY} and phase voltage V_{Rn} against time, assuming a star-connected

resistive load (with proper numerical values on the axes). Also find the THD in the output terminal voltage.
(2+3+7+2+3+4+2 = 23)

4. (a) From concept of fixed voltage space-phasors develop concepts of sectors, sector boundaries, hexagon boundary and explain how theoretically any voltage space-phasor can be obtained through a combination of different switchings in case of SVPWM. Obtain expressions of modulation index and clearly indicate under and over-modulation zones. Derive expressions for switching times t_0, t_x, t_y and t_7 and explain that they stand for. Enlist the switching sequences within the different sectors for a CP (centred-pulse) SVPWM scheme.
(b) A given 3-phse 3-leg SVPWM inverter produces 3-phase balanced output with about 80% fundamental content. The switching frequency is 9.6 kHz. The dc bus voltage is 560V whereas the magnitude of the inverter voltage in the space-vector plane is 335 V.
(i) Evaluate the modulation index.
(ii) Locate any 2 consecutive voltage space phasors in any one sector and evaluate the switching times t_0, t_x, t_y and t_7 in each case.
(iii) Draw the switching logic waveforms of the six devices corresponding to <u>any one</u> of the 2 cases in part (ii) above.
(4+3+4+2 + 2+6+2 = 23)

Group C

5. (a) For a unipolar PWM technique employed on a 4-quadrant DC-DC converter operating under continuous conduction at steady state, derive the relationship between control voltage and DC output voltage. What is the major advantage of using a unipolar PWM over a bipolar PWM strategy employed for controlling the output of this converter? [7+2=9]
(b) In the circuit of the DC-DC converter shown in Fig. KM1, assuming direct duty ratio control, mention how the switching of the two shown IGBT's should be controlled. Assuming continuous conduction and steady state; draw typical waveforms of the important voltages and currents in different parts of the circuit and derive the relationship between the input and output DC voltages. Mention if there is any limit to the maximum duty ratio that can be achieved here with reasons. Explain whether the transformer of the above converter operate with unidirectional core excitation or bidirectional core excitation. [1+9+3+1=14]

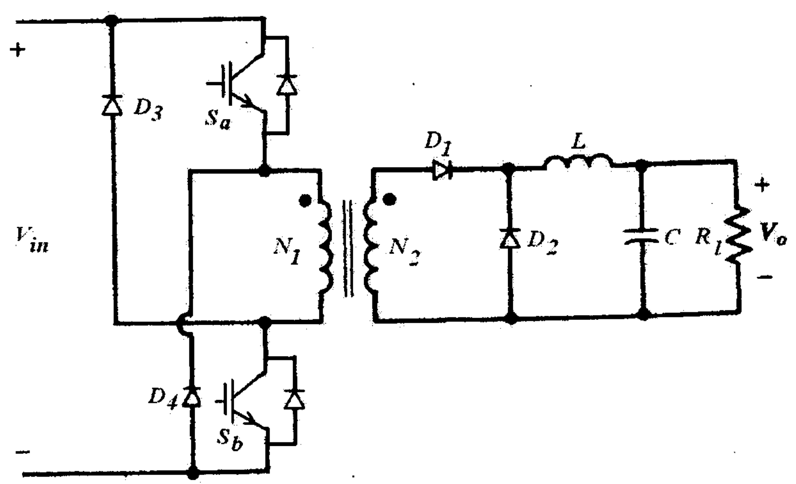

Fig. KM1

6. (a) In a step-up DC-DC converter, consider all components to be ideal. The input DC voltage may vary between 8 V and 16 V, whereas the output DC voltage will be held regulated at 24V. The switching frequency used is 20 kHz and the output DC capacitor is 470 microfarads. Calculate the minimum value of the inductance that will keep the converter operating in a continuous conduction mode if the output power varies between 5W and 30W. [4]
(b) What is discontinuous conduction in a DC-DC converter? Derive the mathematical condition, which when satisfied, will cause a DC-DC buck converter to operate at the boundary of continuous and discontinuous conduction. [2+6=8]
(c) What are the functions of a driver circuit of a power electronic converter? Draw a typical complete bidirectional driver circuit of a IGBT-based half-bridge DC-DC converter and explain the role of its components. [4+7=11]