(Confidential) Ref. No.:

M.E. (Electrical) 1st Semester Final Examination, November 2012

Subject: Power Electronics I

Code No. **EE 906**
Branch: EE
Time: 3 hours Full Marks: 70

(i) The questions are of equal value.
(ii) Answer any ***three full*** questions taking one ***from each Group in the same answerscript***.
(iii) Use graph paper(s) if required.
(iv) One mark reserved for neat and organized answers.

Group A

1. (a) Briefly state the salient features in the construction of power Bipolar Junction Transistor? (b) Discuss the second breakdown phenomena. (c) Draw and explain the turn-off waveform of a power BJT used as a CE switch where the collector is connected to an ideal diode clamped highly inductive load acting as a constant current source (d) Given the circuit in Fig.1, estimate the maximum permissible switching frequency. The freewheeling diode is ideal and the power transistor has the parameters: β=10, $V_{CE(sat)}$ = 1.5 V, $R_{\theta_{j-a}}$ =1°C/W, Tj,max=150°C, $t_{ri} = t_{fi}$ = 260ns, $t_{fv1} = t_{fv2} = t_{rv1} = t_{rv2}$ = 50ns, and $t_{d(on)} = t_{d(off)}$ = 100ns. The BJT is driven by a square wave (50% duty cycle) voltage of variable frequency. Assume I_o = 40 A and V_{CC} = 100 V. (e) What is the requirement of n^- layer in an n-channel power MOSFET (f) What is the disadvantage of this n^- layer?

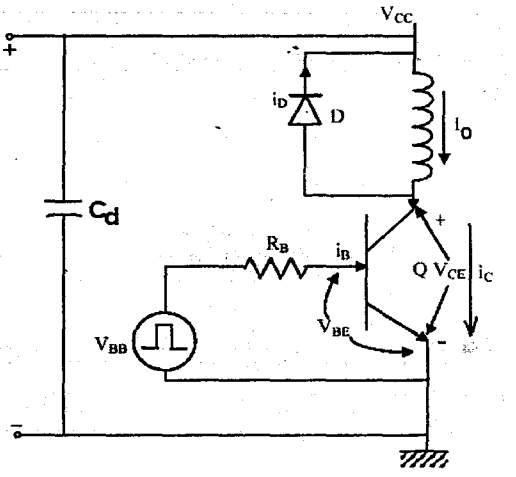

Fig.1 [3+3+5+6+3+3=23]

2. (a)Why it is important to limit $\frac{dv_{ds}}{dt}$ in a power MOSFET? (b) Why it is easier to get parallel operation of power MOSFETs than BJTs (c) Justify the statement that "Models of an IGBT shows that it behaves as a Darlington circuit (MOSFET with BJT) with the $pn^-n^+p^+$ transistor as the main transistor and the MOSFET as the driver" (d) Explain how the conductivity modulation is possible in the n- drift layer in an IGBT (e) What is current tailing problem in an IGBT and how it is prevented in a punch through IGBT structure? (f) How the static latch-up is avoided in an IGBT?

[3+2+5+(4)+(4+2)+3=23]

Group B

3. (a) A 3-phase 3-leg inverter is decided to be operated from a 560 V dc bus following a 180^0 conduction logic at 50 Hz for each switching device. After preparing the appropriate switching sequence table against the different electrical angles, draw with appropriate numerical values, the switching logic wave forms, the output line and phase voltages, the pole voltages (v_{ao} etc.) and the voltage v_{no} (where the symbols "*n*" and "*o*" have their conventional meaning).
(b) With appropriate derivations, comment on the harmonics (including their percent content and Hz values) present in the line and pole voltages. Find the THD in the output line voltage.
(c)Why can we not have more than 180^0 and less than 120^0 conduction in a 3-phase bridge VSI?
(d) For a 3-phase bridge inverter fed from a 560 V DC-link, draw switching logic pulses for a conceptual 150^0 conduction case. Draw the line voltage V_{RY} and phase voltage V_{Rn} against time, assuming a star-connected resistive load (with proper numerical values on the axes). Also find the THD in the output terminal voltage.

[(2+3)+8+2+(2+4+2) = 23]

4. (a) From concept of fixed voltage space-phasors develop concepts of sectors, sector boundaries, hexagon boundary and explain how theoretically any voltage space-phasor can be obtained through a combination of different switchings in case of SVPWM. Obtain expressions of modulation index and clearly indicate under and over-modulation zones. Derive expressions for switching times $\mathbf{t_0}$, $\mathbf{t_x}$, $\mathbf{t_y}$ and $\mathbf{t_7}$ and explain that they stand for. Enlist the switching sequences within the different sectors and on the sector boundaries for a CP (centred-pulse) SVPWM scheme.
(b) A given 3-phase 3-leg SVPWM inverter produces 3-phase balanced output with 85% fundamental content. The switching frequency is 9.6 kHz. The dc bus voltage is 560V whereas the rms value of the output fundamental line voltage is 325 V.
(i) Evaluate the modulation index.
(ii) Locate any 2 consecutive voltage space phasors in any one sector and evaluate the switching times $\mathbf{t_0}$, $\mathbf{t_x}$, $\mathbf{t_y}$ and $\mathbf{t_7}$ in each case.
(iii) Draw the switching logic waveforms of the six devices corresponding to any one of the 2 cases in part (ii) above.

[(4+3+4+2) + (2+6+2) = 23]

Group C

5. Answer all parts:
   a) Explain direct duty-ratio control used in DC-DC converters through a control block diagram.
   b) Draw the power circuit diagram of a DC-DC forward converter employing a flux-resetting circuit using a three-winding transformer.
   c) Derive the input-output voltage relationship of the above-referred forward converter under continuous conduction.
   d) For a duty ratio of about 0.33, draw representative waveforms of the output load current, transformer secondary current, transformer primary voltage, magnetizing current referred to primary, transformer primary current of the above-referred DC-DC forward converter under continuous conduction.
   e) Justify the statement with reasons – "The maximum permissible duty ratio in a DC-DC forward converter employing a three-winding transformer is 0.5".
   f) Explain the working principle of the above-referred DC-DC converter with the help of the power circuit and the waveforms, drawn while answering above questions.

[4+3+3+5+3+5=23]

6. Answer all parts:
   a) Justify the statement with reasons – "The origin of a flyback DC-DC converter is from a DC-DC buck-boost converter."
   b) With the help of power circuit diagrams and waveforms, explain the operation of a Class E DC chopper feeding a DC motor load, operating under unipolar pulse width modulation (PWM).
   c) Draw the typical representative magnetizing flux waveform of the high frequency transformer employed in a push-pull DC-DC converter operating under continuous conduction, when the transformer secondary voltage exhibits a duty ratio of 0.33.
   d) Two diodes out of the four diodes in a single phase diode-based bridge rectifier, meant for power frequency rectification purposes, are mounted on a single heat sink. The rectifier feeds a DC motor load and the load current is continuous and ripple-free and its value is 30 Amps. The threshold voltages of the two diodes are 0.7V and 0.8V respectively and the forward resistances of the diodes are 15 mΩ and 10 mΩ respectively. The worst case junction temperature of any diode should be considered as 150^0C. The ambient temperature can be 45^0C in worst case. The $R_{\theta JC}$ and $R_{\theta CS}$ values of the two diodes are same and are 1.1^0C/W and 0.4^0C/W respectively. Determine the proper $R_{\theta SA}$ value for the heat sink to be selected.

[3+10+3+7=23]