(Confidential) Ref. No. :

M.E. (EE) 2nd Semester Examination, April 2013

Subject : Power Electronics III

Code No. **EE 1014**
Branch: EE
Full Marks : 70

Time : 3 hours

(i) The questions are of equal value. One mark is reserved for neatness and preciseness.
(ii) Answer any ***three*** questions taking only ***one question*** from each group
(iii) Use graph papers, if required, to answer any question(s).

Group A

1. (a) Why scaling operation in software is necessary for a Fixed point DSP?
   (b) What is the range of real numbers that can be represented by Q3.12 format (for a fixed point processors)?
   (c) Explain the procedure to be adopted to get the product of two numbers in Q3.12 format in a 32 bit fixed point processor. . The product should be stored in Q3.12 format.
   (c) Describe the procedure for measurement of speed (using speed encoder) in TMS320LF2407A. (**Programming not required**)

[3 +2+ 3+ 15]

2. (a) Describe the procedure to compute rotor flux angular position using TMS320LF2407A. (**Programming not required**)

   (b) Describe the computational procedure to transform a-b-c frame current to d-q (synchronously rotating frame) current using TMS320LF2407A. (**Programming not required**)

[12+11]

Group – B

3. **a)** Why are resonant converters used only in cases when the input side has d.c. source? What is the unique advantage of application of such converters?
   b) A resonant buck converter using a MOEFET has $L_d = 0.1\ \mu H$ and $C_s = 0.1 \mu F$. The input voltage is 12 V. The converter is intended to feed a 5V, 100 W load with zero-voltage switching (ZVS). Find the operating frequency and the gate signal duty ratio to produce the desired action. Draw the load current profile during the four modes. Derive in brief the necessary analytical expressions and explain the working of the converter. Will ZVS action take place if the load drops to 10 W? Justify with clarity.

c) Draw the circuit diagram of a zero-voltage switching (ZCS) buck converter and briefly explain its working. What are the conditions that are to be satisfied for this resonant converter to successfully work? (3 + 12 + 7)

4. **a)** Draw the typical I-vs-V and Po-vs- V characteristics of a PV array. With the help of the equivalent circuit and otherwise justify why a PV array is considered as a current source rather than a voltage source. What are the effects of the insolation and temperature on the I-vs-V and Po-vs-V characteristics? What are the effects of partial shading on PV arrays?
b) Explain the basic logic of the perturb-observe and the adaptive perturb-observe algorithm used for maximum power point tracking of the dc-dc converter mentioned above. What are the variables to be sensed and what is the quantity to be controlled w.r.t. the converter (devices)?
c) Explain with appropriate circuit diagram and control block diagram, how a standard 3-phase inverter module can be used as a 3-phase interleaved boost chopper sharing one-third current each? Why is this interleaving preferred?
d) Explain with appropriate functional and circuit diagram the operation of a simple 3-level inverter. Prepare appropriate tables and identify how many distinct switching states are possible. Draw the space vector diagram for the different switching states and locate the pivot vectors and null vectors. (5+5+5+8 = 23)

Group –C

5. Answer all parts:
   a) Develop the D-Q transformation based mathematical model of a D-STATCOM.
   b) Hence, draw the control block diagram of the D-STATCOM and explain the control scheme.
   c) Hence, discuss the methodology for finding out the parameters of the controllers employed for the above control block diagram.

(8+8+7=23)

6. Answer all parts:
   a) Discuss the state-space based averaging technique employed to develop the dynamic model of the power stage of a DC-DC converter.
   b) Hence, derive the small-signal transfer function of a DC-DC buck converter, considering the presence of ESR of its capacitor and the loss-representing resistor of its DC choke.

(10+13=23)