(Confidential) Ref. No. :

M.E. (Electrical)
1st Semester Examination, December 2011

Subject : Power Electronics I

Code No. EE 906
Branch: EE
Time : 3 hours Full Marks : 70

(i) The questions are of equal value.
(ii) Answer any ***five*** questions taking any ***two from Group A and three from Group B*** .
(iii)Use graph paper(s) if required.

Group A

1. (a)Why n- drift region is provided in the construction of power Bipolar Junction Transistor? (b) Draw output characteristic of a power BJT and briefly state distinctive features. (c) What is conductivity modulation? (d) A Power BJT is used to switch a diode clamped inductive load carrying 40 A. The supply voltage is 600V dc, switching frequency and duty cycle are 20 kHz and 0.5 respectively. Switching times are as follows. $t_d = 2\mu s$, $t_{ri} = t_{fv1} = 8\ \mu s$, $t_{fv2} = 0$, $t_s = 12\ \mu s$, $t_{fi} = t_{rv2} = 8\ \mu s$, $t_{rv1} = 0$. Calculate switching and conduction losses in the transistor. Justify clearly the assumptions made in the calculation.

(2+4+2+6)

2. (a) Why gate metallization area is extended over drain n- drift region in a power MOSFET? (b) Why p-type body and n+ source layer is shorted through metallic contact in a power MOSFET? (c) Why second breakdown phenomenon is absent in power MOSFET? (d) Explain the operation of MOSFET during drain to source voltage fall times. The MOSFET is used to switch a diode clamped inductive load. (e) A Power MOSFET has the following data Cgs = 800 pF ; Cgd = 150 pF; $g_f = 4$ S; $V_{GS(th)} = 3$V. It is used to switch a clamped inductive load of 20 Amps with a supply voltage $V_D = 200$V. The gate drive voltage is $V_{GG} = 15$V, and gate resistance $R_G = 50\Omega$. Find out the maximum value of $\frac{di_d}{dt}$ and $\frac{dv_{DS}}{dt}$ during turn-on.

(2+2+2+3+5)

3. (a) Explain how a parasitic thyristor is formed in an IGBT. (b) What are PT and NPT IGBTs, c)Explain why during turn-off, the current tailing is observed in IGBT (d) Explain how the ON state current is mostly diverted through the MOSFET section of the IGBT? (e) Explain why latch-up condition can occur in an IGBT (f) How latch-up can be avoided?

(2+2+3+2+2+3)

Group B

4. (a) A 3-phase fully controlled bridge rectifier is fed from a 415 V, 50 Hz supply. The source side inductance per phase is 12 mH. Neglecting source resistance and rectifier device drops, for continuous and level load current of 100A and a firing angle of $\alpha = 30^\circ$.
   (i) evaluate the mean output voltage after deriving necessary relations.
   (ii) draw the load voltage and the input line current.

(b) In the above rectifier determine the THD and the input power factor if the source inductance is neglected.
(c) How will the input current waveform look if the load is shunted by a heavy capacitor? Justify your answer.

(5+4+3+2)

5. (a) From first principles of switching converter and utilizing KCL and KVL develop through appropriate derivations, the configuration of a boost-converter. Develop expressions for instantaneous and average value of different significant input and output variables. Draw waveforms for an assumed switching function. Show how device ratings cane be derived from such an elementary approach in case the input is 5V and the output 15 V and the load power requirement is 50W.

(b) In a dc-dc boost chopper, V_i = 8-16 V dc (fluctuates) and V_o =24 V dc. Given that f_s = 10 k Hz, C = 470 μF, calculate the minimum value of L that will keep the converter working in a continuous-conduction mode if the output power has to be $P_o \geq 5$ W. Assume all components to be ideal and draw all significant waveforms.

(8+6)

6. (a) A 3-phase 3-leg inverter is decided to be operated from a 560 V dc bus following a 180° conduction logic at 50 Hz for each switching device. After preparing the appropriate switching sequence table against the different electrical angles draw the switching logic wave forms, the output line and phase voltages, the pole voltages (v_{ao} etc.) and the voltage v_{no} if "*n*" and "*o*" refer respectively to the neutral point of the star connected load and the center-point voltage of the usual two capacitors connected in series across the dc-bus (with proper numerical values on the axes).
(b) With appropriate derivations, comment on the harmonics (including their percent content and Hz values) present in the line and pole voltages.
(c)Why can we not have more than 180° and less than 120° conduction in a 3-phase bridge inverter?

(2+3+7+2)

7. Explain the concept of SVPWM. From concept of fixed voltage space phasors develop concepts of sectors, sector boundaries, hexagon boundary and explain how theoretically any voltage space phasor can be obtained through a combination of different switchings. Obtain expressions of modulation index and clearly indicate under and over-modulation zones. Derive expressions for switching times t_0, t_x, t_y and t_7 and explain that they stand for. Enlist the switching sequences within the different sectors and on the sector boundaries.(4+4+4+2)

8. (a) For a 3-phase bridge inverter fed from a 560 V DC-link, draw switching logic pulses and space vectors for a conceptual 150° conduction case. Draw the line voltage V_{RY} and phase voltage V_{Rn} against time, assuming a star-connected resistive load (with proper numerical values on the axes).

(b) A given 3-phse 3-leg SVPWM inverter produces 3-phase balanced output with 85% fundamental content. The switching frequency is 9.6 kHz. The dc bus voltage is 560V whereas the rms value of the output fundamental line voltage is 325 V.
(i) Evaluate the modulation index.
(ii) Locate at least 4 probable voltage space phasors in a given sector and evaluate the switching times t_0, t_x, t_y and t_7 in each case.

(4+2+2+6)