First Year ME (ICE), First Semester Examination 2013

Advanced Computer Architecture (ICE-905/4)

Full Marks-70 **Time: 3 hours**

Answer any 7 questions

1. a) Initially $t0 contains 0x23456789. After the following program is run, what value does $s0 contain in the big-endian system and the little-endian system?

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sw $t0, 0($0)
lb $s0, 1($0)
```

   b) How will the larger constants be loaded into the registers in MIPS?
   c) Explain R-type format in MIPS?
   d) Why is 'MIPS direct addressing mode' called 'Pseudo-direct Addressing'?
   e) In direct addressing mode, the jump target address (JTA) is 0x04000A0, calculate the 26 bits address. 2+2+2+2+2

2. a) What is exception in MIPS? What are the functions of the cause register and exception PC in exception? What is the instruction address of exception handler? Explain the steps of the exception.
   b) A program runs in 10 sec on computer A, which has a speed of 400 MHz clock. A designer wants to build a new machine B, which will run this program in 6 sec. He can use new technology to substantially increase the clock rate. This will affect the rest of the CPU design, causing B to require 1.2 times as many clock cycles as A for the same program. What clock rate should we tell the designer to target? 1+2+1+3+3

3. a) There are two implementations (A and B) of the same instruction set architecture (ISA). For some program, A has clock cycle time of 10 ns, CPI of 2.0 and B has clock cycle time of 20 ns, and CPI of 1.2. Which machine is faster for this program, and by how much? If two machines have the same ISA, which the quantity will always be identical?
   b) Two compilers are being tested for 100 MHz machine with the following 3 classes of instructions.' A', 'B', 'C' instruction needs 1 cycle, 2 cycles, and 3 cycles respectively. Compiler 1 consists of 5M 'A' instructions, 1M 'B' instructions, and 1M 'C' instructions. Compiler 2 consists of 10M A instructions, 1M B instructions, 1M C instructions. Which sequence has higher MIPS? Which sequence has lower execution time?
   c) What is Amdahl's Law? 5+4+1

4. a) Design a 4 bit CLA adder using propagate and generate block.
   b) Construct 16 bit look ahead with 2 levels of abstraction.
   c) Write express for delay of an *N*-bit carry-look-ahead adder with *k*-bit blocks.
   d) Compare the delay of 32-bit ripple-carry, and carry-look-ahead adders. The carry-look-ahead adder has 4-bit blocks. Assume that each two-input gate delay is 100 ps and the full adder delay is 300 ps. 4+2+2+2

5. a) Design 32 bit Arithmetic Logic Unit (ALU) for implementing AND, OR, add, sub, beg, slt
   b) Explain & draw the simple single cycle data path for the MIPS architecture executing the basic instructions load/store word, ALU operation and branch operation. 5+5
6. a) What are the problems with single cycle design?
   b) How do you calculate the clock period for single cycle and multi-cycle design?
   c) Draw the block diagram implementation for Multi-cycle approach. 3+4+3
7. a) Draw the abstract model of pipelined data path.
   b) How do you handle data hazards in pipeline data path?
   c) Discuss the solutions of control hazard in the pipeline data path? 3+3+4

8. a) Define Instruction-Level and Processor-Level-parallelism.
   b) What are the different types of processor organizations according to Flynn's classification?
   c) Describe Single bus, shared memory multiprocessing (SMP). 4+2+4

9. a) Discuss the use of assert statements and the severity types used in VHDL.
   b) Design a 3 Bit comparator using VHDL models.
   c) State the types of delays incorporated in signal assignment statements used in VHDL? Discuss with suitable examples. 3+4+3
10. a) State the differences in application of functions and procedures in VHDL
   b) Design a serial in parallel out register (3 bit) using VHDL model.
   c) State the application and advantages of Signals and Variables in relation to VHDL with suitable examples. 2+5+3