First Year ME (ICE), First Semester Examination 2012

Advanced Computer Architecture (ICE-905/4)

Full Marks-70 **Time: 3 hours**

Answer any 7 questions

1. a) Translate the following assembly language statement into machine language.
   i) add $s0, $s1, $s2
   ii) sub $t0, $t3, $t5
   (Given, machine code for add=32, sub=34, $s1=17, $s2=18, $s0=16, $t0=8, $t3=11, $t5=13)
   b) In MIPS programs, at which starting address are the MIPS Instructions normally stored?
   c) Why is the 'MIPS direct addressing mode' called 'Pseudo-direct Addressing'?
   d) If the JTA of the jal instruction is 0x004000A0, derive the 26-bit address field (addr) of this jal instruction.
   e) What is MIPS address space? 3+1+2+3+1

2. a) What is Amdahl's Law?
   b) A program runs in 100 seconds on a machine, with multiply responsible for 80%. How much do we have to improve the speed of multiplication if we want the program to run 4 times faster? How about making it 5 times faster?
   c) Suppose we enhance a machine to make all floating-point instructions five times faster. If the execution time of some benchmark before the floating-point enhancement is 10 seconds, what will the speedup be if half of the 10 seconds is spent executing floating-point instructions?
   2+(2+2)+4

3. a)What is the delay for the following types of 64-bit adders? Assume that each two-input gate delay is 150 ps and that a full adder delay is 450 ps.
   (i) a ripple-carry adder
   (ii) a carry-lookahead adder with 4-bit blocks
   (iii) a prefix adder
   b) Design a shifter that always shifts a 32-bit input left by 2 bits. The input and output are both 32 bits. Explain the design in words and sketch a schematic.
   6+4

4. a) Implement the following functions using a single 16 x 3 ROM. Use dot notation to indicate the ROM contents.
   i) $X = AB + BC'D + A'B'$
   ii) $Y = AB + BD$
   iii) $Z = A + B + C + D$
   b) Specify the size of a ROM that you could use to program each of the following combinational circuits. Is using a ROM to implement these functions a good design choice? Explain why or why not.
   i) a 16-bit adder/subtractor with *C*in and *C*out
   ii) an 8 x 8 multiplier 6+4

5. a) Write different control inputs in tabular form for single cycle data path implementing MIPS Architecture.
   b) Calculate the delay for the instructions {add, sub, and, or, slt, sw, lw, beq, j}.
   5+5

6. a) What are the problems with single cycle design?
   b) How do you calculate the clock period for single cycle and multi-cycle design?
   c) Draw the block diagram implementation for Multi-cycle approach.

   3+3+4

7. a) Draw the abstract model of pipelined data path.
   b) How do you handle data hazards in pipeline data path?
   c) Discuss the solutions of data hazard in the following codes? 3+3+4

```
add $s0, $s2, $s3
and $t0, $s0, $s1
or $t1, $s4,$s0
sub $t2, $s0, $s5
```

8. a) How do you calculate Miss and hit rates?
   b) Suppose a program has 2000 data access instructions (loads or stores), and 1250 of these requested data values are found in the cache. The other 750 data values are supplied to the processor by main memory or disk memory. What are the miss and hit rates for the cache?
   c) Find the number of set and tag bits for a direct mapped cache with 1024 (2^{10}) sets and a one-word block size. The address size is 32 bits.
   d) In Memory hierarchy (CPU← L_1 cache← L_2 cache← main memory) with two levels of cache, the access times for the L_1 cache, L_2 cache, and main memory are 1, 10, and 100 cycles respectively. Assume that the L_1 and L_2 caches have miss rates of 5% and 20%, respectively. What is the average memory access time (AMAT)?
   e) Suppose a cache has a block size of four words. How many main memory accesses are required by the following code when using each write policy: write-through or write-back?

```
sw $t0, 0x0($0)
sw $t0, 0xC($0)
sw $t0, 0x8($0)
sw $t0, 0x4($0)
```

   2+1+2+2+3

9. a) Define Instruction-Level-parallelism and processor-level-parallelism.
   b) What are the different types of Processor organizations according to Flynn's classification?
   c) What are the four potential advantages of SMP processor? 2+4+4

10. a) What are Packages ? How are these formed and used in VHDL models?
    b) "Processes can be executed in the absence of sensitivity list": Explain
    c) Design a 4 Bit even parity generator using VHDL models.

    3+3+4 = 10

11. a) Briefly define the configuration declaration and configuration specifications in context of VHDL with suitable examples.
    b) What are the types of delays incorporated in signal assignment statements used in VHDL? State with suitable examples.
    c) State the differences in application of functions and procedures in VHDL.

    4+2+4 = 10