ME (ICE) 2nd Semester Examination, 2012
ICE 1005/7: CAD for VLSI

Time: 3 Hr

FM: 70

Answer any FIVE.

1. How can you realize a chip design problem from different domains viz. behavioral, structural, and physical. Explain. "In DSM regime, VLSI physical design problem has become interconnect centric". Justify.   3+3+3+5

2. What are the primary challenges in advanced digital design today? Explain. How many types of signals can you find in a VLSI circuit? How do the phases in layout design find importance in clock synchronization problem today?   6+2+6

3. How is test verification carried out? What is the objective of formal verification of a design? What is the role of technology mapping during logic synthesis? What is the purpose of using feedthrough in standard cell based design? What are primary advantages of FPGA based design over ASIC?   4+2+3+2+3

4. What is optical proximity correction? How does it help in layout designing? What are design rules? Why are these used for? What is the purpose of using wells and substrate taps during the fabrication process? Explain.   2+3+2+2+5

5. Classify different types of partitioning algorithms. How KL algorithm may be extended for unequal sized blocks and unequal sized elements? Explain how the global optima can be achieved by using simulated annealing during partitioning?   3+5+6


6.
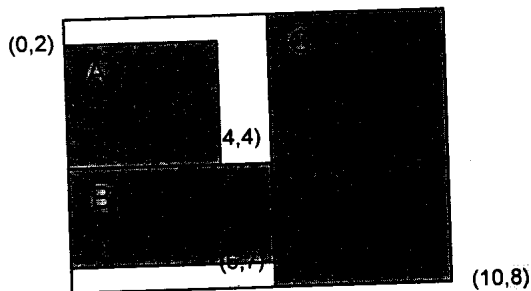
  a. Consider the above placement of three blocks A, B and C. Compute
     i. Center to center Euclidean wirelength
     ii. Center to center HPWL
     iii. % of deadspace
  b. Clearly mention the difference between floorplanning and placement problem.
  c. In MILP formulation of the floorplanning problem clearly mention
     i. Non-overlapping constraints for fixed blocks
     ii. How can you define Integer variables
     iii. A general problem formulation   6+2+6

7. What is Grid routing? What are the different algorithms used for grid routing? Explain different steps in Lee's algorithm for maze routing. What is the space complexity of this algorithm? Mention different improvements for this. Explain the grid graph model with a clear example.

1+2+4+1+2+4
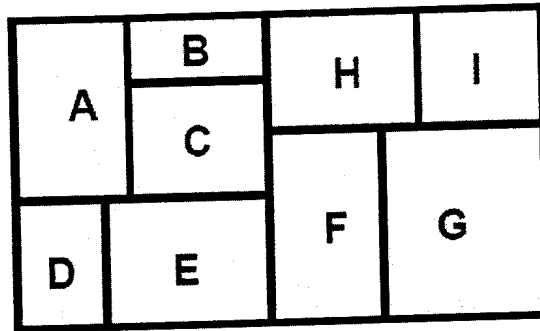
8. What is a slicing tree? Is the above floorplan sliceable? If yes, give its slicing tree representation. What are the inputs, requirements, and objectives of the placement problem? How the problem varies at different levels of design? What different modeling techniques are used for wire length estimation of multi-terminal nets during placement? Clearly explain with neat diagram.

2+1+2+3+3+3